Curriculum Vitae[1] *of*

SRINIVAS KATKOORI

Associate Professor
Department of Computer Science and Engineering
University of South Florida

RESEARCH INTERESTS

Internet-of-Things (IoT), Emerging Technologies, In-Memory Computing, Smart Embedded Systems (Smart Transportation, Smart Health-care, Smart Caregiving), Hardware Security, High Level Synthesis, Low Power Synthesis, FPGA Based Synthesis, Radiation Tolerant CAD for FPGAs, Evolutionary Algorithms, IC Reliability, Virtual Reality.

EDUCATION

- *Doctor of Philosophy, Computer Engineering* *1992–1998*
  Department of ECECS, University of Cincinnati, Cincinnati.
  University Graduate Scholarship (UGS) for the entire duration of doctoral studies.
  1997-98 Outstanding Doctoral Dissertation, Honorable Mention, ECECS Dept.
- *Bachelor of Engineering, Electronics and Communication Engineering* *1988 – 1992*
  Department of Electronics and Communication Engineering (ECE),
  Osmania University, Hyderabad, India.
  Admission by state wide Engineering entrance (EAMCET) test. Stood in top 1% of test takers.
  Passed in first class with distinction.

WORK EXPERIENCE

- *Associate Professor* *Aug. 2004 – present*
  Department of Computer Science and Engineering,
  University of South Florida, Tampa, Florida.
- *Sabbatical Leave* *Aug. 2005 – Dec 2005*
  Bio-Inspired Technologies & Systems
  NASA Jet Propulsion Labs (JPL), Pasadena, CA.
- *Assistant Professor* *Aug. 1997 – July 2004*
  Department of Computer Science and Engineering,
  University of South Florida, Tampa, Florida.

[1] As of September 30, 2023.

- *Research Assistant* *1993–95, 1996–97*
  Digital Design Environments Laboratory (DDEL),
  Department of Electrical and Computer Engineering and Computer Science (ECE&CS),
  University of Cincinnati, Cincinnati, Ohio.

AWARDS & HONORS

- **Program Chair**, IEEE International Symposium on Smart Electronic Systems (iSES), 2023, Ahmedabad, December 2023.
- **Program Co-Chair**, GLSVLSI 2023, Knoxville, June 2023.
- **Associate Editor 2022-present**, IEEE Transactions on Consumer Electronics
- **Best Paper Award**, IEEE International Symposium on Smart Electronic Systems (iSES), 2022.
- **Best Paper Nomination**, 5th IFIP International Internet-of-Things (IoT) Conference, Netherlands, 27-28 October 2022.
- **General Co-Chair**, 8th IEEE International Symposium on Smart Electronic Systems (iSES), Warangal, India, December 2022.
- **General Co-Chair**, 5th IFIP International Internet-of-Things (IoT) Conference, Netherlands, 27-28 October 2022.
- **Associate Editor**, IEEE Consumer Electronics Magazine, Jan 2021 - Present.
- **Best Paper Award**, IEEE International Symposium on Smart Electronic Systems (iSES), 2020.
- **Program Co-Chair**, 4th IFIP International Internet-of-Things (IoT) Conference, Netherlands, 4-5th November 2021.
- **Program Co-Chair**, 39th International Conference on Consumer Electronics (ICCE), 10-12 January 2021.
- **Program Chair, IEEE Computer Society Symposium on VLSI**, Tampa, FL, 2021.
- **Program Chair**, 3rd IFIP International Internet-of-Things (IoT) Conference, Netherlands, 5-6th November 2020.
- **Program Co-Chair**, Intl. Conference on Consumer Electronics (ICCE), 10-12 January 2021.
- **General Chair**, 2nd IFIP International Internet-of-Things (IoT) Conference, Tampa, FL, 31st October - 1st November 2019.
- **General Chair**, 5th IEEE International Symposium on Smart Electronic Systems (iSES), Rourkela, India, 16-18th, December 2019.
- **Best Paper Nomination** at IEEE Asian Hardware Oriented Security and Trust (AsianHOST), 2018.
- **2017-18 USF Outstanding Graduate Faculty Mentor Award, Honorable Mention.**
- **Vice Chair** of International Federation for Information Processing (IFIP) Working Group 10.5 (Design and Engineering of Electronic Systems), 2015-2020.
- **Best Paper Nomination** at 2014 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC).
- **2013 USF Jerome Krivanek Distinguished Teacher Award**.
- **2012 SIGDA Service Award**, "*In Appreciation for Contributions To ACM/SIGDA*."
- **2009 Certificate of Recognition** by USF Computer Science & Engineering Department, "*For his leadership and outstanding service as Graduate Program Director*," for service from May 2006 to April 2009.

- **2008 Elevation to Senior Member Status**, Association of Computing Machinery (ACM).
- **2007 Certificate of Appreciation, Alfred P. Sloan Foundation**, "*In appreciation for your commitment to advancing under-represented minority students in mathematics, science and engineering and for your leadership in the Alfred P. Sloan Foundation's Minority Ph.D. Program.*"
- **2007-2008 USF Outstanding Undergraduate Teaching Award**.
- Recognition of IEEECS student chapter with "**2003 Outstanding Chapter Award,**" under Dr. Katkoori's Advisorship.
- **2005 National-level IEEE-USA Professional Achievement Award**. *Nominated by IEEE Florida West Coast Section.*
- **2005 Outstanding Engineering Educator Award**, IEEE Florida Council Award (Region 3), *Nominated by the IEEE Florida West Coast Section (FWCS).*
- **Member, Sigma Xi**, The Scientific Research Society, 2004 (By Invitation).
- **2004 Elevation to Senior Member Status**, IEEE.
- **Best Paper Nomination** at 2003 International Conference on Asian and South-Pacific Design Automation Conference (ASP-DAC).
- **2003 University of South Florida Outstanding Faculty Research Achievement Award**.
- **2001 Faculty Early Career Development Grant (CAREER), National Science Foundation**, Design Automation Program, to conduct research for five years on *"Interconnect centric High Level Synthesis in Deep-Sub-Micron Regime."*
- **1997-98 Outstanding Doctoral Dissertation, Honorable Mention**, Department of Electrical and Computer Engineering and Computer Science, University of Cincinnati.
- **Awarded sponsorship** to attend NATO Advanced Study Institute Workshop entitled *"Low Power in Deep Submicron Electronics,"* Italy, August 20-30, 1996.
- **Research Assistantship**, Digital Design Environments Laboratory, University of Cincinnati, *June 1993-95, 1996-97*
- **University Graduate Scholarship (UGS)**, University Of Cincinnati, *Fall 1992 - 1997*
- **Third Place** at Under-Graduate level **AP State Mathematics Olympiad, India**, 1990.

RESEARCH GRANTS *&* CONTRACTS

- National Science Foundation *Jan 2023 - Dec 2027*
  Title: CyberCorps Scholarship for Service: Cybersecurity Research and Education for Service in Government (CREST)
  Amount: *$3,702,920*
  Role: PI
- Department of Education *Sep 2022 - Aug 2023*
  Title: Project HaHa: Low-Cost Hands-on Hardware Security Education
  Amount: *$205,000*
  Role: Co-PI
- Missile Defense Agency (MDA) (SBIR sub-contract) *Dec 2020 - Dec 2022*
  Title: Cellulose Based Flexible Solid-State High Power and High Energy Supercapacitor
  Amount: *$273,555*
  Role: Co-PI

- Florida High Tech Corridor (Partner: PolyMaterialsApp Inc.) *June 2020 - June 2021*
  Title: Feasibility Study of a Portable Hazardous Chemical Detection System
  Amount: *$20,000*
  Role: PI
- American Association of Nurse Practitioners *Aug 2020 - Sep 2021*
  Title: Collaborative Research: Intervention to Facilitate Communication Between Suddenly Speechless Patients and Healthcare Providers
  Amount: *$5,000*
  Role: Co-PI
- National Science Foundation *May 2020 - Apr 2025*
  Title: SATC:EDU: Improving Student Learning through Gamified Embedded System Security Challenges
  Amount: *$499,727*
  Role: Co-PI
- National Science Foundation (NSF) *2019*
  Title: I-Corps: A Smart Technology for Child Safety
  Amount: *$50,000*
  Role: PI
- National Science Foundation (NSF) *April 2018 – April 2021*
  Title: PAfitME - Use of eHealth to Personalize Exergame Prescriptions
  Amount: *$50,000*
  Role: Co-PI
- DARPA TTO *Sep 2016 - Sep 2019*
  Title: Threshold-Defined Switches for Novel Logic Engines
  Amount: *$625K (approx.)*
  Role: PI. Sub-contract to Penn. State Univ (Dr. Swaroop Ghosh)
- Department of Defense *2016*
  Title: Multi-tier Optimization of 5G Heterogeneous Networks
  Amount: *$50K (approx.)*
  Role: CSE: S. Katkoori (co-PI) EE: R. D. Gitlin (PI), H. Arslan, and S. Kose.
- Florida Department of Transportation *2014 – 2017*
  Title: Naturalistic Bicyling Behavior Pilot Study
  Amount: *$349,721*
  Role: CSE: S. Katkoori (co-PI) CUTR: P-S. Lin (PI), A. Kourtellis, and L. Cruse.
- Florida High Tech Corridor Council (FHTCC) *June 2014 – May 2015*
  Title: Miniature Wireless High Definition Video Imaging Devices for In Vivo Minimally Invasive Surgery
  Amount: *$50,000*
  Role: CSE: S. Katkoori (co-PI); EE: R. Gitlin (PI).
- Tampa Hillsborough Expressway Authority *July 2013 – Dec 2014*
  Title: Automated Vehicles: A Catalyst for Tampa Bay
  Amount: *$125,000*
  Role: CSE: S. Katkoori (co-PI) CUTR: J. Bittner (PI), S. Reich (co-PI), and several others.
- USF Student Green Energy Fund *Aug 2013 – Dec 2014*
  Title: Smart Parking Guidance System

Demonstration Project
Amount: *$500,000*
Role: CUTR: S. Hendricks (PI)
CSE: S. Katkoori and R. Kasturi, *supervisors for the the team working on camera based real-time decal identification problem.*

- USF Student Green Energy Fund *Jan 2013 – Dec 2014*
  Title: Event Based Scheduling Optimization
  for Building Air Handlers
  Amount: *$28,000*
  Role: Co-PI. PI: R. Meana (Graduate Student).
- National Science Foundation, CCF *2010 - 2011*
  Title: CADathlon 2010: International Graduate
  Student Progg. Contest in EDA
  Amount: *$10,000*
  Role: PI. Co-PIs: S. Pasricha (CSU), J. Roy, and S. Banerjee.
- National Science Foundation, *2006 - 2008*
  Title: *CRI: Infrastructure acquisition for*
  sub-100 nano VLSI research
  Amount: *$215,023*
  Role: Co-PI. PI: S. Bhanja (EE), Co-PIs: H. Zheng, N. Ranganathan, and V.K. Jain (EE).
- NASA Jet Propulsion Labs (JPL) RHESE Project *2006*
  Title: *Hardware and Software Implementations of Intelligent and Evolvable Algorithms*
  Amount: *$100,000*
  Role: PI. *Sub-contract to USF by NASA JPL.*
- I4 High Tech Corridor Initiative *2003-2004*
  (Industry Partner: Honeywell, Inc, Clearwater)
  Title: *STMR based Software Tool and Application*
  Development Targeted to HRSC Board
  Amount: *$45,000*
  Role: PI.
- I4 High Tech Corridor Initiative *2002-2003*
  (Industry Partner: Honeywell, Inc, Clearwater)
  Title: *Requirements Analysis for an Automatic Synthesis*
  Framework for Honeywell Reconfigurable Space Computer
  Amount: *$25,000*
  Role: PI.
- National Science Foundation, Design Automation Program *2001 - 2005*
  Faculty Early Career Development Grant (CAREER)
  Title: *CAREER: Interconnect-centric High-Level Synthesis*
  in Deep Sub-Micron (DSM) Regime
  Amount: *$310,000*
  Role: PI.
- I4 High Tech Corridor Initiative *2000-2001*
  (Industry Partner: Honeywell, Inc, Clearwater)
  Title: *High-Throughput and Low-Power Implementations of*

Space-Based Radar Algorithms on RC Hardware
Amount: *$150,000*
Role: PI.

- Honeywell Incorporation *2001-2002*
  SASSO/CSO Academic Initiatives IR&D Program 2001
  Title: *SEU-tolerant Synthesis for FPGA based Space Systems*
  Amount: $11,000
  Role: PI.
- Honeywell Space Systems Inc. *2000-2001*
  SASSO/CSO Academic Initiatives IR&D Program 2000
  Title: *Reconfigurable Computing Architectures for Payload Processing (Signal & Datastream) Applications*
  Amount: $13,000
  Role: PI.
- Design Automation Graduate Scholarship *1999 - 2000*
  Design Automation Conference Council
  Title: *RT-level Route-and-Place Design Methodology for Delay and Power Optimization in DSM Regime*
  Amount: *$24,000*
  Proposed for Stelian Alupoaei and Udaykumar Anumalachetty
- Research & Creative Scholarship, *1997 - 98*
  University of South Florida Research Council and
  Division of Sponsored Programs.
  Title: *Interconnect Power Analysis and Optimization in High Level Synthesis Framework*
  Amount: *$7,500.00*

PROFESSIONAL MEMBERSHIPS

- American Association for Advancement of Science (AAAS)
- Association for Computing Machinery (ACM)
- ACM Special Interest Group on Design Automation (SIGDA)
- The Institute of Electrical and Electronics Engineers (IEEE)
- IEEE Computer Society
- IEEE Circuits and Systems Society
- Sigma Xi, The Scientific Research Society

TEACHING EXPERIENCE

- Associate Professor, Department of Computer Science & Engineering, University of South Florida, August 2004 – *present*.
- Assistant Professor, Department of Computer Science & Engineering, University of South Florida, August 1997 – July 2004.
- Teaching Assistant, Department of ECE&CS, University of Cincinnati, 1995–1996.
- Completed *"Advanced Teaching Techniques,"* course offered bi-annually by the Department of Advanced Teaching Institute, University of Cincinnati, Winter 1994.

- Attended a Teaching Workshop entitled *"Preparing Future Faculty,"* Division of Research and Advanced Studies, University of Cincinnati, May 1996.

LIST OF ALL COURSES TAUGHT AT USF

Undergraduate Courses

- Computer Organization (Gate Course)
- Computer Logic Design (Core Course)
- Computer Architecture (Core Course)
- Computer System Design (Core Course)
- CMOS VLSI Design (Core Course)
- Digital Circuit Synthesis (Senior Elective)
- CMOS VLSI Testing (Senior Elective)
- Advanced Computer Architecture (Senior Elective)
- Hardware-Oriented Security & Trust (Senior Elective)
- Advanced Embedded Systems (Senior Elective)
- IoT System Design (Senior Elective)
- Secure IoT (Senior Elective)

Graduate Courses

- Principles of Computer Architecture (Core Course)
- CMOS VLSI Design
- Low Power CMOS VLSI Design
- Digital Circuit Synthesis
- Testing & Fault Tolerance in Digital Systems
- Hardware-Oriented Security & Trust
- Advanced Embedded Systems

COURSE OFFERINGS (SEMESTER-BY-SEMESTER)

Undergraduate Core Courses

- *Computer Organization (CDA 3103)*
  Offered in: Fall 2009.
- *Computer Logic Design (EEL 4705 / CDA 3201)*
  Offered in: Fall 1999, Fall 2000. Note: Course number changed in Fall 2000.
- *Computer Organization & Architecture (CDA 4100)*
  Offered in: Summer 1998, Spring 1998, Spring 1999, Summer 2000, Fall 2002, Fall 2003.
- *Computer System Design (CDA 4203) & Lab (CDA 4203L)*
  Offered in: Fall 1997, Fall 2007.
- *CMOS VLSI Design (CIS 4213) & Lab (CDA 4213L)*
  Offered in: Spring 2004, Spring 2005, Fall 2006, Fall 2008, Fall 2009.

Undergraduate Senior Electives

- *Advanced Computer Architecture*
  Offered in: Spring 2000.

- *Digital Circuit Synthesis*
  Offered in: Spring 2002, Spring 2003, Fall 2004, Spring 2008.
- *CMOS VLSI Testing*
  Offered in: Spring 2007.

Graduate Core Courses

- *Principles of Computer Architecture (EEL 6764 001)*
  Offered in: Fall 1998, Spring 1998, Fall 1999, Spring 2000.

Graduate Electives

- *CMOS VLSI Design*
  Offered in: Spring 2000, Fall 2000, Fall 2001, Spring 2003, Spring 2004, Spring 2005, Fall 2006, Fall 2009, Spring 2009.
- *Low Power CMOS VLSI Design and CAD*
  Offered in: Fall 1998, Spring 2000, Spring 2001, Spring 2002.
- *Advanced Computer Architecture*
  Offered in: Spring 2000.
- *Digital Circuit Synthesis*
  Offered in: Spring 2002, Fall 2003, Fall 2004, Fall 2005, Spring 2008.
- *Testing & Fault Tolerance in Digital Systems (EEL 6706 001)*
  Offered in: Spring 2007.

VLSI CAD TOOL RELATED EXPERTIZE

- *Physical Design*: CADENCE Tool Suite (Virtuoso), MAGIC, HSPICE, Nanosim, Fire & Ice, Celtic Crosstalk Analyzer.
- *Logic Synthesis*: SIS, Synopsys Tool Suite
- *High-level Synthesis*: Developed AUDI (Automatic Design Instantiation), an in-house high-level synthesis system in C language. This system is extended by several PhD and MS students for their thesis work.
- *FPGA Related Tools*: Xilinx ISE, Embedded Design Kit (EDK).
- *Hardware Description Languages (HDLs)*: VHDL and Verilog.
- *Automatic Translators/Parsers*: lex, flex, yacc, bison, ANTLR.
- *Other Languages*: C, C++, Java, Unix shell scripting, Awk, sed.

GRADUATE STUDENT SUPERVISION (Graduated 19 PhDs, 43 MS)

- **PhD Theses supervised**
  Total: 19 Doctoral degrees awarded.

  1. Dr. Rajeev Joshi Summer 2016 – Summer 2023
     Dissertation Title: *Optimization Techniques for Machine Learning Inference and Near Memory Image Processing in Hardware for Highly Constrained IoT Edge Nodes*
     First Employment: TBA.

2. Dr. Omkar Dokur — Spring 2019 – Spring 2023
   Dissertation Title: *V2V and V2I Based Safety and Platooning Algorithms for Connected and Autonomous Vehicles*
   First Employment: TBA.
3. Dr. Matthew Lewandowski — Fall 2013 – Summer 2021 (part-time)
   Dissertation Title: *Secure VLSI Hardware Design Against Intellectual Property (IP) Theft and Cryptographic Vulnerabilities*
   First Employment: USF Tech Support.
4. Dr. Love Kumar Sah — Summer 2016 – Fall 2020
   Dissertation Title: *Micro-architectural Countermeasures for Control Flow and Misspeculation Based Software Attacks*
   First Employment: Tenure Track Assistant Professor, ECE Department, West Northern England (WNE) University, MA.
5. Dr. Vishalini Laguduva — January 2018 – Summer 2020
   Dissertation Title: *Machine Learning for the Internet of Things: Applications, Implementation and Security*
   First Employment: Visiting Assistant Professor, Oklahoma State University, Stillwater, OK.
6. Dr. Sheikh Ariful Islam — Fall 2014 – Summer 2020
   Dissertation Title: *Behavioral and RT-level Synthesis of Secure Nano VLSI Digital ASIC Designs*
   First Employment: Tenure Track Assistant Professor, CS Department, University of Texas, Rio Grande Valley, TX.
   Recognized with 2020 USF Outstanding Dissertation Award
7. Dr. Rekha Govindraj — Summer 2016 – Summer 2018
   (co-advised with Dr. Swaroop Ghosh, Penn. State University)
   Dissertation Title: *Emerging Non Volatile Memory Technologies for Computing and Security*
   First Employment: Apple, Inc, San Jose, CA.
8. Dr. Evren Bozgeyikli — Fall 2013 – Fall 2016
   (Co-advised with Dr. A. Raij, EE, USF)
   Dissertation Title: *Locomotion in Virtual Reality for Room Scale Tracked Areas*
   First Employment: Assistant Professor, Univ. of Arizona, Tucson, AZ. Starting Fall 2017.
9. Dr. Lal Bozgeyikli — Fall 2013 – Fall 2016
   (Co-advised with Dr. A. Raij, EE, USF)
   Dissertation Title: *Virtual Reality Serious Games for Training Individuals with Autism Sprectrum Disorder: Design Considerations*
   First Employment: Assistant Professor, Univ. of Arizona, Tucson, AZ. Starting Fall 2017.
10. Dr. Santosh Aditham — Fall 2012 – Spring 2017
    (Co-advised with Dr. N. Ranganathan, CSE, USF)
    Dissertation Title: *Mitigation of Insider Attacks for Data Security in Distributed Computing Environments*
    First Employment: Juniper Networks, San Jose, CA.

11. Dr. Shilpa Pendyala — Fall 2009 – Fall 2015
    Dissertation Title: *Synthesis Techniques for Sub-threshold Leakage and NBTI Optimization in Digital VLSI Systems*
    First Employment: Intel, Portland, OR.
12. Dr. Soumyaroop Roy — Summer 2005 – Summer 2010
    (Co-advised with Dr. N. Ranganathan, CSE, USF)
    Dissertation Title: *Architecture and Compiler Support for Leakage Reduction Using Power Gating in Microprocessors*
    First Employment: AMD, Texas, Austin.
13. Dr. Pradeep Fernando — Summer 2005 – Fall 2009
    Dissertation Title: *Genetic Algorithm Based Design and Optimization of VLSI ASICs and Reconfigurable Hardware*
    First Employment: Post-doc, EPFL, Lausanne, Switzerland.
14. Dr. Hariharan Sankaran — Spring 2003 - Fall 2008
    Dissertation Title: *High-Level Synthesis Framework for Crosstalk Minimization in VLSI ASICs*
    First Employment: Synopsys, Bangalore, India.
15. Dr. Vyas Krishnan — Spring 2003 - Fall 2008
    Dissertation Title: *Temperature And Interconnect Aware Unified Physical And High Level Synthesis*
    First Employment: Assistant Professor, St. Leo University, Tampa, FL.
16. Dr. Suvodeep Gupta — Spring 2002 - Fall 2004
    Dissertation Title: *Behavioral and RT-level Cross-talk Estimation and Optimization in VLSI ASICs*
    First Employment: Intel, Phoenix, AZ.
17. Dr. Hao Li (Co-advised with Dr. W-K. Mak) — Fall 1999 - Fall 2004
    Dissertation Title: *Low Power Technology Mapping and Performance Driven Placement for Field Programmable Gate-Arrays*
    First Employment: Assistant Professor, CSE, University of North Texas at Denton.
    Currently working for Synopsys Inc, San Jose, CA.
18. Dr. Chandramouli Gopalakrishnan — Spring 2000 - Fall 2003
    Dissertation Title: *High Level Techniques for Estimation and Optimization of Leakage Power of VLSI ASICs*
    First Employment: CADENCE, Noida India.
    Currently working for Synopsys Inc, Bangalore, India.
19. Dr. Stelian Alupoaei — Summer 1999 - Spring 2003
    Dissertation Title: *Interconnect-centric Macrocell Placement Approaches in DSM Regime*
    First Employment: Intel, Portland, OR.

- **PhD Theses currently supervising**
  Total: 2 (2 PhD candidates)

1. Neilesh Shambhu — Summer 2023 – current
   Topic Area: Connected and Autonomous Vehicles
2. Lakshmi Kavya Kalyanam — Spring 2018 – current
   Topic Area: Machine Learning in Hardware

- **MS Theses supervised**
  Total: 43 MS degrees awarded.

  1. Gustavo Olenscki — Fall 2021 – Summer 2023
     Thesis Title: Vehicle-to-Vehicle (V2V) and Vehicle-to-Infrastructure (V2I) Based Intersection Movement Assist, Lane Change Assist, and Rear Traffic Jam Formation Safety Applications.
  2. Ruchitha Chinthala — Fall 2019 – Spring 2022
     (co-advised with Dr. Carmen Rodriguez, College of Nursing, USF)
     Thesis Title: An Internet of Medical Things (IoMT) Approach for Remote Assessment of Head and Neck Cancer Patients. **(1) USF Best Thesis Award. (2)Honorable Mention, USF Nomination for Graduate Thesis Award at Conference of Southern Graduate Schools (CSGS).**
  3. Sai Praneeth Sagi — Fall 2017 – Summer 2020
     (co-advised with Dr. Wilfrido Moreno, EE Department, USF)
     Thesis Title: Implementation of SR Flip-Flop Based PUF on FPGA for Hardware Security
  4. Lakshmi Kavya Kalyanam — Fall 2018 – Summer 2020
     Thesis Title: Edge Computing for Deep Learning-Based Distributed Real-time Object Detection on IoT Constrained Platforms at Low Frame Rate.
  5. Rajeev Joshi — Fall 2016 – Summer 2020
     Thesis Title: Novel Bit-sliced In-Memory Computing Based VLSI Architecture for Fast Sobel Edge Detection in IoT Edge Devices. *Continued for Doctoral Degree.*
  6. Sri Varsha Polnati — Fall 2017 – Spring 2019
     Thesis Title: An Efficient Runtime CFI Check for Embedded Processors to Detect and Prevent Control Flow Based Attacks.
  7. Venkata Lakshmi Bhargavi Gurram — Spring 2018 – Fall 2018
     Thesis Title: Gate Level Probabilistic Simulation Based Hardware Trojan Susceptability Analysis of Combinational Circuits.
  8. Varshini Kandikonda — Fall 2016 – Summer 2018
     Thesis Title: A Key Based Obfuscation and Anonymization of Behavioral VHDL Models.
  9. Rohit Prasad Challa — Spring 2017 – Summer 2018
     Thesis Title: SR Flip-flop based Physically Unclonable Function (PUF) for Hardware Security *First Employment:* Qualcomm, San Diego.
  10. Vinaya Malleypally — Fall 2016 – Spring 2018
      Thesis Title: Parallelizing Tabu Search Based Optimization Algorithm on GPUs.
  11. Soundarya Revoori — Fall 2016 – Summer 2017
      Thesis Title: Computing the Rectilinear Crossing Number of K_{n+1} from K_n.
  12. Radhakrishna Aluru — Summer 2016 – Fall 2016
      (co-advised with Dr. Swaroop Ghosh, Penn. State University)
      Thesis Title: Voltage Droop Analysis and Mitigation in a STTRAM Last Level Cache.
  13. Deepak Reddy Voleti — Summer 2016 – Fall 2016
      (co-advised with Dr. Swaroop Ghosh, Penn. State University)
      Thesis Title: Methodologies to Exploit ATPG Tools for De-camouflaging.
  14. Ithihasa Reddy — Summer 2016 – Fall 2016

(co-advised with Dr. Swaroop Ghosh, Penn. State University)
Thesis Title: Threshold Voltage Defined Switches and Gates to Prevent Reverse Engineering.

15. Raghav Sharma Fall 2015 – Fall 2016
(co-advised with Dr. Rich Gitlin, EE, USF)
Thesis Title: High Level Modeling and Synthesis of OFDM on FPGA.
16. Janardhan B. Karri Fall 2014 – Fall 2015
(Co-advised with Dr. P-S. Lin, CUTR, USF)
Thesis Title: Low Power Real-time Video and Audio Embedded System Design for Naturalistic Bicycle Study.
17. Omkar Dokur (co-advised with Dr. W. Moreno (EE)) Spring 2014 – Fall 2015
(Co-advised with Dr. W. Moreno, EE, USF)
Thesis Title: Embedded System Design of a Real-time Parking Guidance System.
18. Robert P. O'Brien Spring 2014 – Spring 2015
(Co-advised with Dr. Meredeth Rowe, College of Nursing, USF)
Thesis Title: Embedded System Design for Real-time Monitoring of Solitary Alzheimer's Patients at Home.
19. Daniel Ashley Spring 2012 –
(Co-advised with Dr. R. Alqesami, MechE, USF)
Thesis Title: Using Embedded Systems to Determine the Configuration of a Static Wheelchair Mounted Robotic Arm.
20. Matthew Johnson Fall 2012 – Fall 2013
Thesis Title: Design of an Advanced Lighting Measurement System for Roadway Safety.
21. Noureddine Elmehraz Fall 2011 – Summer 2013
Thesis Title: Design of a Highly Portable Data Logging Embedded System for Naturalistic Motorcycle Study.
Continued for a doctoral degree.
22. Richard Meana Fall 2011 – Summer 2013
Thesis Title: Approximate Sub-Graph Isomorphism for Watermaking Finite State Machine Hardware.
Continued for a doctoral degree.
23. Matt Lewandowski Fall 2011 – Spring 2013
Thesis Title: A Novel Method for Watermarking Sequential Circuits.
Continued for a doctoral degree.
24. Chris Bell Fall 2011 – Spring 2013
Thesis Title: A Multi-Parameter Functional Side Channel Analysis Method for Hardware Trojan Detection in Untrusted FPGA Bitstreams.
Continued for a doctoral degree.
25. Mark La Spina Spring 2009 – Spring 2010
Thesis Title: Parallel Genetic Algorithm Engine on an FPGA.
26. Nagalakshmi Subramanya Spring 2007 – Summer 2008
(Co-advised student with Dr. R. Tripathi, CSE, USF)
Thesis Title: Study of FPGA implementation of entropy norm computation for IP data streams.
27. Soumyaroop Roy Fall 2003 – Summer 2005

(Co-advised with Dr. N. Ranganathan, CSE, USF)
Thesis Title: A Compiler Based Leakage Reduction Technique by Power-Gating Functional Units in Embedded Microprocessors
Continued for a doctoral degree.

28. Pradeep Fernando Fall 2003 – Summer 2005
Thesis Title: Genetic Algorithm Based Two-Dimensional and Three-Dimensional Floorplanning for VLSI ASICs.
Continued for a doctoral degree.
29. Supriya Sunki Fall 2003 – Summer 2005
Thesis Title: Performance optimization in three-dimensional programmable logic arrays (PLAs).
30. Sujana Kakarla Fall 2003 – Spring 2005
Thesis Title: Partial Evaluation Based Triple Modular Redundancy for SEU Mitigation.
31. Hariharan Sankaran Fall 2001 – Summer 2005
Thesis Title: System level energy optimization for location aware computing.
Continued for a doctoral degree.
32. Ranganath Gopalan Fall 2002 – Spring 2005
Thesis Title: Behavioral Synthesis of Low Leakage Pipelined Datapaths.
First Employment: Intel, San Jose, CA.
33. Viswanath Daita Fall 2002 – Fall 2004
(Co-advised with Dr. Wilfredo Moreno, EE, USF)
Thesis Title: Behavioral VHDL Implementation of Coherent Digital GPS Signal Receiver.
34. Umadevi Kailasam Fall 2001 – Spring 2004
Thesis Title: High Level VHDL Modeling of a Low-Power ASIC for a Tour Guide.
First Employment: Golden Gate Technology, San Jose, CA.
35. Anulekha Bilhanan Fall 2001 – Spring 2004
(Co-advised with Dr. John Heine, Moffitt Cancer Research Institute)
Thesis Title: Implementation of Mammograph analysis algorithms on FPGA.
First Employment: Fischer Imaging Inc, Denver, CO.
36. Praveen Bamini Fall 2001 - Fall 2003
Thesis Title: Implementation of a Speech Synthesis System.
First Employment: Verizon, Tampa, FL.
37. Praveen Samudrala Fall 2001 - Spring 2003
Thesis Title: Selective Triple Modular Redundancy based Single Event Upset (SEU) Mitigation for FPGAs
First Employment: SpaceMicro Corporation, San Diego.
Currently working for Qualcomm, San Diego.
38. Joe Rogers (Co-advised with Dr. Ken Christensen) Fall 1998– Summer 2002
Thesis Title: Network Traffic Study of Internet2.
First Employment: Academic Computing, USF.
39. Suvodeep Gupta Fall 1999 - Spring 2002
Thesis Title: Force-directed Scheduling for Dynamic Power Optimization.
Continued for a doctoral degree.
40. Gayatri Garudadri

Project Title: Register Transfer (RT) Level Simulation of the MIPS Pipelined Processor in JAVA.

41. Chandramouli Gopalakrishnan Fall 1997 - Fall 2000
    Thesis Title: Power Optimization via Input Transformations.
    Continued for a doctoral degree.
42. Smitha Myneni Fall 1997 - Spring 2000
    Thesis Title: Development of Accurate Power Simulator using hierarchical VHDL Specification.
    First Employment: Intel Corporation, Santa Clara, CA.
43. Ananth Durbha Summer 1998 - Fall 1999
    Thesis Title: A Novel Route-and-Place RTL Design Methodology for Interconnect Optimization in DSM Regime.
    First Employment: Intel Corporation, Santa Clara, CA.

- **MS Theses currently supervising**
  Total: 3 MS Students

1. Raaga Sai Somesula Summer 2022 – current
   Topic: Machine Learning on IoT Edge Nodes.
2. Susmitha Boyidapu Fall 2022 – current
   Topic: Smart IoT Healthcare.
3. Ramakrishna Kanneganti Summer 2023 – current
   Topic: Low Power VLSI Design.

UNDERGRADUATE SUPERVISION

- Anjaly Kuruvilla and Ryan Schmidt, Senior Project "PCB Implementation of a Solar Powered Embedded System for an Intelligent STOP Sign", Spring 2014.
- Robert P. O'Brien, Honors Thesis, Fall 2012.
- James Muldoon, Senior Project, Spring 2012.
- Matthew Johnson, Senior Project, Spring 2012.
- Daniel Ashley, REU Project, Fall 2011.
- Richard Meana, Senior Project, Fall 2011.
- Matthew Lewandowski, Senior Project, Fall 2011.
- Chris Bell, REU Project, Spring 2011.
- Matthew Lewandowski, REU Project, Spring 2011.
- Richard Meana, REU Project, Spring 2011.
- Qi Zhao, Senior Project, Fall 2009.
- Khris Martinez, Senior Project, Fall 2009.
- Rey Cablong, Senior Project, Fall 2009.
- Andrew Mast, Senior Project Spring 2008.
- Jamie Montelegre, Senior Project, Spring 2008.
- Luke Jenkins, Senior Project, Spring 2008.
- Bhavna Kumar, REU, Spring 2005.
- Ryan Mabry, REU, Summer 2004.
- Billy Klerk, REU, Summer 2004.

- Andrew White, Senior Project, Spring 2003.
- Jeremy Ramos, Senior Project & McNairs Scholar, Fall 2000.

PATENTS

1. *Method and apparatus for creating circuit redundancy in programmable logic devices*, Praveen K. Samudrala, Srinivas Katkoori, and Jeremy Ramos. US Patent No. 6,963,217. Issued Nov. 8 2005.
   Abstract: A method for reducing circuit sensitivity to single event upsets in programmable logic devices, involves identifying single event upset sensitive gates within a single event upset sensitive sub-circuit of a programmable logic device as determined by the input environment and introducing triple modular redundancy and voter circuits for each single event upset sensitive sub-circuit so identified.
2. *SR Flip-flop Based Physical Unclonable Functions for Hardware Security*, Srinivas Katkoori, Rohith Prasad Challa, and Sheikh Ariful Islam. US Patent No. 11,537,755 B1. Issued Dec. 27 2022
   Abstract: The present disclosure presents various systems and methods for implementing a physical unclonable function device. One such method comprises providing an integrated circuit having a plurality of set / reset flip flop logic circuits, wherein each of the set / reset flip flop logic circuits enters a meta-stable state for a particular input sequence. The method includes varying circuit parameters for each of the plurality of set / reset flip flop logic circuits to account for manufacturing variations in the set / reset flip flop logic circuits and enable generating a stable but random output in response to the particular input sequence. Thus, by applying the particular input sequence to the integrated circuit, a unique identifier for the integrated circuit can be derived from an output response of the plurality of set / reset flip flop logic circuits.

INVITED TALKS

- Drexel University, Philadelphia, PA.
- Arizona State University, Tempe, AZ.
- University of Tennessee, Knoxville, TN.
- Rochester Institute of Technology, Buffalo, NY.
- University of Texas, El Paso, TX.
- Honeywell Space Systems, Clearwater, FL.
- Osmania University, Hyderabad, India.
- Navigational Electronics Research & Training Unit (NERTU), Osmania University, Hyderabad, India.
- National Institute of Technology (NIT, formerly REC), Warangal, India.
- AFRL Workshop on Radiation Hardening by Design, Albuquerque, NM.
- University of Southern California, CA.
- Jet Propulsion Laboratory, CalTech, Pasadena, CA.
- IBM, Seminar on Selective Triple Modular Redundancy.
- Center for Ocean Technology, College of Marine Science, USF.
- University of North Texas, Denton.
- Georgia Institute of Technology, Atlanta.

- Univ. of Southern California, LA.
- Seminar Speaker, Center for Communication & Signal Processing (CCSP), USF.
- Communications Network Group, USF.

BOOKS

1. S. Katkoori and S. A. Islam (Editors), "Behavioral Synthesis for Hardware Security," Springer, 1st edition, 2022. ISBN 3030788407.
2. S. Katkoori, O. Dokur, and G. Olenscki (Editors), "Connected Vehicles - Algorithms, Frameworks, and Safety Studies," Springer, under preparation.

BOOK CHAPTERS

1. S. Pendyala and S. Katkoori, "Interval Arithmetic and Self Similarity Subthreshold Leakage Optimization in RTL Datapaths" In IFIP International Federation for Information Processing 2015 L. Claesen et al. (Eds.): VLSI-SoC 2014, IFIP AICT 464, pp. 75–94, 2015. **Best Paper Candidate. Invited Book Chapter.**
2. M. A. Zaman, R. Joshi, and S. Katkoori, "Optimizing Performance and Energy Overheads Due to Fanout in In-Memory Computing Systems," In: Bombieri N., Pravadelli G., Fujita M., Austin T., Reis R. (eds) VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms. VLSI-SoC 2018. IFIP Advances in Information and Communication Technology, vol 561. Springer, Cham. **Invited Book Chapter.**
3. "Behavioral Synthesis of Key-Obfuscated RTL IP," Sheikh Ariful Islam and Srinivas Katkoori, in Behavioral Synthesis for Hardware Security, Editors Katkoori and Islam, 2022, pp. 17 – 42, Springer.
4. "State Encoding Based Watermarking of Sequential Circuits, Using Hybridized Darwinian Genetic Algorithm," Matthew Lewandowski and Srinivas Katkoori, in Behavioral Synthesis for Hardware Security, Editors Katkoori and Islam, 2022, pp. 177 – 203, Springer.
5. "Hardware Trojan Localization: Modeling and Empirical Approach," Sheikh Ariful Islam and Srinivas Katkoori, in Behavioral Synthesis for Hardware Security, Editors Katkoori and Islam, 2022, pp. 205 – 231, Springer.

LIST OF PUBLICATIONS

Total: 152 (Journal Articles: 30, Conference Papers: 122)

PEER REVIEWED JOURNAL ARTICLES (30)

1. R. Joshi, Md A. Zaman, and S. Katkoori, "Fast Sobel Edge Detection for IoT Edge Devices," **Springer Nature Computer Science**, Volume 3, No. 4, Pages. 302, Springer. 2022

2. Md A. Zaman, R. Joshi, and S. Katkoori, "Early Design Space Exploration Framework for Memristive Crossbar Arrays," **ACM Journal on Emerging Technologies in Computing Systems**, Vol. 18, Issue 2, April 2022.

3. S. Katkoori, S. A. Islam, and S. Kakarla "Partial Evaluation based Triple Modular Redundancy for Single Event Upset Mitigation," **Integration**, Vol. 77, pp. 167-179, March 2021.

4. V. R. Laguduva, S. Katkoori, and R. Karam, "Machine Learning Attacks and Countermeasures for PUF-Based IoT Edge Node Security," **Springer Nature Computer Science**, Vol. 1, No. 282, 2020.

5. S. A. Islam, L. K. Sah, S. Katkoori, "A Framework for Hardware Trojan Vulnerability Estimation and Localization in RTL Designs," **Springer Journal of Hardware and Systems Security (HaSS)**, 4, pp. 246-262, 2020.

6. S. Pendyala, S. A. Islam, and S. Katkoori, "Interval Arithmetic and Self-Similarity Based RTL Input Vector Control for Datapath Leakage Minimization," **ACM Transactions on Design Automation of Electronic Systems (TODAES),** No. 54, September 2020.

7. S. A. Islam, L. K. Sah, and S. Katkoori, "High-Level Synthesis of Key Obfuscated RTL IP with Design Lockout and Camouflaging," **ACM Transactions on Design Automation of Electronic Systems (TODAES),** No. 6, October 2020.

8. E. Bozgeyikli, A. Raij, S. Katkoori, and R. Dubey, "Locomotion in Virtual Reality for Room Scale Tracked Areas," **International Journal on Human Computer Studies (JHCS),** Vol. 122, Pages 38-49, Feb. 2019.

9. R. Govindaraj, S. Ghosh and S. Katkoori, "CSRO-Based Reconfigurable True Random Number Generator Using RRAM," **IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)**, vol. 26, no. 12, pp. 2661-2670, Dec. 2018.

10. R. Govindaraj, S. Ghosh and S. Katkoori, "Design, Analysis and Application of Embedded Resistive RAM based Strong Arbiter PUF," **IEEE Transactions on Dependable and Secure Computing (TDSC)**. 2018. doi: 10.1109/TDSC.2018.2866425

11. L. Bozgeyikli, A. Raij, S. Katkoori and R. Alqasemi, "A Survey on Virtual Reality for Individuals with Autism Spectrum Disorder: Design Considerations," **IEEE Transactions on Learning Technologies (TLT)**, vol. 11, no. 2, pp. 133-151, 2018.

12. L. Bozgeyikli, E. Bozgeyikli, S. Katkoori, A. Raij, R. Alqasemi, "Effects of Virtual Reality Properties on User Experience of Individuals with Autism." **ACM Transactions on Accessible Computing** Vol. 11 No. 4 Pages, 22:1-22:27 (2018).

13. S. Pendyala, S. A. Islam, and S. Katkoori, "Gate Level NBTI Optimization in Combinational Circuits with Input Vector Cycling," **IEEE Transactions on Emerging Topics in Computing (TETC),** 2018. doi: 10.1109/TETC.2018.2799739.

14. L. Bozgeyikli, E. Bozgeyikli, A. Raij, R. Alqasemi, S. Katkoori, and R. Dubey, "Vocational Rehabilitation of Individuals with Autism Spectrum Disorder with Virtual Reality," **ACM Transactions on Accessible Computing (TACCESS),** Vol. 10, No. 2, April 2017, Page(s): 5:1 - 5:25.

15. H. Sankaran and S. Katkoori, "Simultaneous Scheduling, Allocation, Binding, Re-ordering, and Encoding for Crosstalk Pattern Minimization during High Level Synthesis," **IEEE Transactions on VLSI Systems (TVLSI)**, Volume 19, Issue 2, Feb. 2011, Page(s): 217 - 226.

16. S. Roy, N. Ranganathan, and S. Katkoori, "State-Retentive Power Gating of Register Files in Multicore Processors Featuring Multithreaded In-Order Cores," **IEEE Transactions on Computers (TC)**, Volume 60, Issue 11, Nov. 2011 Page(s): 1547 - 1560

17. V. Krishnan and S. Katkoori, "TABS: Temperature-Aware Layout Driven Behavioral Synthesis," **IEEE Transactions on VLSI Systems (TVLSI)**, Volume 18, Issue 12, 2010, Page(s): 1649 - 1659

18. P. Fernando and S. Katkoori, D. Keymeulen, R. Zebulum, and A. Stoica, "A Customizable FPGA IP Core Implementation of a General Purpose Genetic Algorithm Engine," **IEEE Transactions on Evolutionary Computation (TEC)**, Volume 14, Issue 1, 2010, Page(s):133 - 149.

19. S. Roy, N. Ranganathan, and S. Katkoori, "A Framework For Power-Gating Functional Units in Embedded Microprocessors," **IEEE Transactions on VLSI Systems (TVLSI)**, Volume 17, Issue 11, Nov. 2009 Page(s):1640 - 1649.

20. K. Vyas and S. Katkoori, "A Genetic Algorithm for Design Space Exploration of Datapaths during High Level Synthesis," **IEEE Transactions on Evolutionary Computation (TEC)**, Volume 10, Issue 3, June 2006 Page(s):213 - 229.

21. S. Gupta and S. Katkoori, "Intra Bus Crosstalk Estimation Using Word-Level Statistics," **IEEE Transactions on Computer-Aided Design of ICs and Systems (TCAD)**, Volume 24, Issue 3, March 2005 Page(s):469 - 478.

22. P. K. Samudrala, J. Ramos, and S. Katkoori, "Selective Triple Modular Redundancy (STMR) Based Single Event Upset (SEU) Tolerant Synthesis for FPGAs," **IEEE Transactions on Nuclear Science (TNS)**, Volume: 51 , Issue: 5 , Oct. 2004, Pages: 2957-2969.

23. S. Alupoaei and S. Katkoori, "Ant Colony System Application for Macrocell Overlap Removal," **IEEE Transactions on VLSI Systems (TVLSI)**, Volume: 12 , Issue: 10 , Oct. 2004 Pages:1118 - 1123.

24. S. Alupoaei and S. Katkoori, "Net Clustering Based Constructive and Iterative Improvement Approaches for Macro-cell Placement," **Journal on VLSI Signal Processing (JVSP)**, Vol. 37, No. 1, May 2004, pp. 151-163.

25. H. Li, W. K. Mak, and S. Katkoori, "Power Minimization Algorithms for LUT Based FPGA Technology Mapping," **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Vol. 9, No. 1, January 2004, pp. 33-51.

26. C. Gopalakrishnan, S. Katkoori, and S. Gupta, "Power Optimization Using Input-based Transformations," Vol. 150, No. 3, May 2003, **IEE Proceedings - Computers and Digital Techniques (IEE CDT)**, pp. 133-142.

27. S. Alupoaei and S. Katkoori, "Net-Based Force-directed Macrocell Placement for Wirelength Optimization," **IEEE Transactions on VLSI Systems (TVLSI)**, Vol. 10, No. 6, December 2002, pp. 824-835.

28. R. Vemuri, S. Katkoori, M. Kaul, and J. Roy, "An Efficient Hierarchical Register Optimization Algorithm for High Level Synthesis from Behavioral Specifications," **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Vol. 7, No. 1, pp. 189-216, January 2002.

29. S. Katkoori and R. Vemuri, "Architectural Power Estimation Based on Behavioral Level Profiling," pp. 255-270, Vol.7, No. 3, **Journal on VLSI Design (JVLSI)**, 1998.

30. N. Kumar, S. Katkoori, L. Rader and R. Vemuri, "Profile-Driven Behavioral Synthesis for Low Power VLSI Systems," **IEEE Design & Test of Computers, Fall Issue**, pp.70-84, 1995.

REFEREED CONFERENCES
(122 Papers, 7 Best Paper Nominations, 3 Best Paper Awards)

1. L. K. Kalyanam and S. Katkoori, "Sigmoid-based Neuron Pruning Technique for MLPs on IoT Edge Devices," The First International Conference on Cyber Physical Systems, Power Electronics, and Electric Vehicles (ICPEEV), Sept. 28-30. 2023. **Accepted.**

2. R. Joshi, R. S. Somesula, and S. Katkoori, "Edge-Driven Intelligence: A Hybrid Machine Learning Strategy for IoT Edge Nodes," The First International Conference on Cyber Physical Systems, Power Electronics, and Electric Vehicles (ICPEEV), Sept. 28-30. 2023. **Accepted.**

3. L. K. Kalyanam, R. Joshi, and S. Katkoori. "Layer-wise Filter Thresholding Based CNN Pruning for Efficient IoT Edge Implementations" 2023 IFIP International Internet of Things Conference (IFIP IoT), November 2-3. 2023. **Accepted**

4. R. Joshi, L. K. Kalyanam, and S. Katkoori. "Simulated Annealing Based Area Optimization of Multilayer Perceptron Hardware for IoT Edge Devices," 2023 IFIP International Internet of Things Conference (IFIP IoT), November 2-3. 2023. **Accepted.**

5. R. Joshi, R. S. Somesula, and S. Katkoori. "Empowering Resource-Constrained IoT Edge Devices: A Hybrid Approach for Edge Data Analysis," 2023 IFIP International Internet of Things Conference (IFIP IoT), November 2-3. 2023. **Accepted.**

6. R. S. Somesula, R. Joshi and S. Katkoori, "On Feasibility of Decision Trees for Edge Intelligence in Highly Constrained Internet-of-Things (IoT)," 33rd ACM GLSVLSI, June 5-7, 2023.

7. R. Joshi, L. K. Kalyanam, and S. Katkoori, "Area Efficient VLSI ASIC Implementation of Multilayer Perceptrons," 2023 International VLSI Symposium on Technology, Systems and Applications (VLSI TSA), Ambassador Hotel Hsinchu, Taiwan, April 17-20. 2023. Accepted.

8. O. Dokur, G. Olenscki, and S. Katkoori, "An Edge Computing Approach for Autonomous Vehicle Platooning," IFIP IoT Conference, 2022, Pages 332-349. **Best Paper Nomination.**

9. M. A. F. Amador, B. Olney, S. Katkoori, and R. Karam, "Comprehensive Open-source SCA Course Modules for Hands-on IoT Security Education," IFIP IoT Conference 2022, Pages 125-139.

10. S. Miryala, G. Carini, G. Deptuch, J. Huang, S. Katkoori, P. Maj, S. Mandal, Y. Ren, Md. A. Zaman, "Design and Challenges of Edge Computing ASICs on Front-End Electronics," ISQED 2022, 19-27

11. S. Miryala, Md A. Zaman, S. Mittal, Y. Ren, G. Deptuch, G. Carini, S. Zohar, S. Yoo, J. Fried, J. Huang, and S. Katkoori, "Peak Prediction Using Multi Layer Perceptron(MLP) for Edge Computing ASICs Targeting Scientific Applications," ISQED 2022. Pages 1-6.

12. G. Olenscki, O. Dokur, and S. Katkoori, "Intersection Movement Assist and Lane Change Assist V2V Warnings with DSRC-based Basic Safety Messages," iSES 2022, 718-723.

13. O. Dokur, G. Olenscki, S. Katkoori, "Platoon Formation Based on DSRC Basic Safety Messages," IEEE iSES 2022, 700-705. **Best Paper Award.**

14. O. Dokur and S. Katkoori, "CARLA Connect: A Connected Autonomous Vehicle (CAV) Driving Simulator," 2022 IEEE International Symposium on Smart Electronic Systems (iSES), Warangal, India, 2022, pp. 656-659.

15. O. Dokur, G. Olenscki, and S. Katkoori, "Slow Moving Vehicle, Do Not Pass, and Stationary Vehicle V2V Warnings Based on DSRC Basic Safety Messages," IEEE iSES 2022, 694-699.

16. G. Singh, S. Abdullah, S. R. Patri, S. Katkoori, "Object Detection and Classification in FWMAVs for Smart Pollination," IEEE iSES 2022, 524-527.

17. R. Joshi, L. K. Kalyanam, and S. Katkoori, "Simulated Annealing Based Integerization of Hidden Weights for Area-Efficient IoT Edge Intelligence," IEEE iSES 2022, 427-432.

18. L. K. Kalyanam, R. Joshi, and S. Katkoori, "Range Based Hardware Optimization of Multilayer Perceptrons with RELUs," IEEE iSES 2022, 421-426.

19. R. Karam, S. Katkoori, M. M. Kermani, "Improving Student Learning in Hardware Security, Project Vision, Overview, and Experiences," IEEE iSES 2022, 297-301.

20. R. Chinthala, S. Katkoori, C. S. Rodriguez, M. J. Mifsud, "An Internet of Medical Things (IoMT) Approach for Remote Assessment of Head and Neck Cancer Patients," IEEE iSES 2022, 124-129.

21. T. P. Kumar, G. Supriya, P. Papnoi, S. R. Patri, S. Katkoori, "Low Power IoT Soil Moisture Sensor Node for Smart Irrigation, " IEEE iSES 2022, 107-111.

22. O. Dokur and S. Katkoori, "Vehicle-to-Infrastructure based Algorithms for Traffic Light Detection, Red Light Violation, and Wrong-Way Entry Applications," IEEE iSES 2022, 25-30

23. O. Dokur and S. Katkoori, "Three Connected V2V Applications Based on DSRC Basic Safety Messages," ICVVE 2022. Pages 1-6.

24. S. Abdullah, P. Appari, S. R. Patri, S. Katkoori, "Smart Agriculture using Flapping-Wing Micro Aerial Vehicles (FWMAVs)," 4th IFIP Internet-of-Things Conference. **Best Paper Award. 1 out of 33 submissions.**

25. R. Podeti, S. R. Patri, S. Katkoori, and P. Muralidhar, "ReOPUF: Relaxation Oscillator Physical Unclonable Function for Reliable Key Generation in IoT Security," 4th IFIP Internet-of-Things Conference.

26. M. Lewandowski and S. Katkoori, "Enhancing PRESENT-80 and Substitution-Permutation Network Cipher Security with Dynamic "Keyed" Permutation Networks," 2021 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Tampa, FL, USA, 2021, pp. 350-355.

27. L. K. Sah, S. A. Islam, and S. Katkoori, "Defending Misspeculation-based Cache Probe Attacks Using Variable Record Table," International Symposium on Quality of Electronic Design (ISQED), 2021, pp. 408-413, doi: 10.1109/ISQED51717.2021.9424259.

28. L. K. Kalyanam, V. Ramnath, S. Katkoori, and H. Zheng, "A Distributed Framework for Real Time Object Detection at Low Frame Rates with IoT Edge Nodes," IEEE International Symposium on Smart Electronic Systems (iSES), 2020. **Best Paper Award. 3 out of 70 papers are recognized.**

29. R. Joshi, A. Zaman, and S. Katkoori, "Novel Bit-Sliced Near-Memory Computing Based VLSI Architecture for Fast Sobel Edge Detection in IoT Edge Devices," IEEE International Symposium on Smart Electronic Systems (iSES), 2020.

30. S. A. Islam, L. K. Sah and S. Katkoori, "Analytical Estimation and Localization of Hardware Trojan Vulnerability in RTL Designs," 2020 21st International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, 2020, pp. 149-154.

31. S. A. Islam and S. Katkoori, "SafeController: Efficient and Transparent Control-Flow Integrity for RTL Design," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2020, pp. 270 - 275.

32. V. Laguduva and S. Katkoori, "A Smart IoT System for Continuous Sleep State Monitoring," Midwest Symposium on Circuits and Systems (MWSCAS), 2020 pp. 241 - 244.

33. M. A. Zaman, R. Joshi, and S. Katkoori, "High Level Modeling of Memristive Crossbar Arrays," 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2020, pp. 524 - 529.

34. L. K. Sah, S. Polnati, S. A. Islam, and S. Katkoori, "Basic Block Encoding Based Run-time CFI Check for Embedded Software," IFIP VLSI-SoC Conference, 2020.

35. M. A. Zaman, R. Joshi, and S. Katkoori, "Analysis of Radiation Impact on Memristive Crossbar Arrays," 11th IEEE Latin American Symposium on Circuits and Systems (LASCAS), 25-28th February 2020, San Jose, Costa Rica.

36. V. Lagudava, S. Mahmud, S. Aakur, R. Karam, and S. Katkoori, "Dissecting Convolutional Neural Networks for Efficient Implementation on Constrained Platforms," The 33rd International Conference on VLSI Design, 4-8 January 2019, Bengaluru, India, pp. 149 - 154.

37. V. Laguduva, S. Aakur, S. Katkoori, "Latent Space Modeling for Cloning Encrypted PUF-based Authentication," 2nd IFIP International IoT Conference. A Confluence of Many Disciplines. IFIP IoT 2019. IFIP Advances in Information and Communication Technology, vol 574. Springer, Cham.

38. M. Lewandowski and S. Katkoori, "Lightweight Countermeasure to Differential-Plaintext Attacks on Permutation Ciphers," 2nd IFIP International IoT Conference, 2nd IFIP International IoT Conference. A Confluence of Many Disciplines. IFIP IoT 2019. IFIP Advances in Information and Communication Technology, vol 574. Springer, Cham.

39. S. A. Islam, L. K. Sah and S. Katkoori, "DLockout: A Design Lockout Technique for Key Obfuscated RTL IP Designs," 2019 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), Rourkela, India, 2019, pp. 17-20.

40. L. K. Sah, S. Ariful Islam and S. Katkoori, "Variable Record Table: A Run-time Solution for Mitigating Buffer Overflow Attack," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, TX, USA, 2019, pp. 239-242.

41. R. P. Challa, S. Ariful Islam and S. Katkoori, "An SR Flip-Flop based Physical Unclonable Functions for Hardware Security," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, TX, USA, 2019, pp. 574-577.

42. V. Laguduva, S. A. Islam, S. Aakur, S. Katkoori and R. Karam, "Machine Learning Based IoT Edge Node Security Attack and Countermeasures," 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Miami, FL, USA, 2019, pp. 670-675.

43. M. Lewandowski and S. Katkoori, "A Darwinian Genetic Algorithm for State Encoding Based Finite State Machine Watermarking," 20th International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, 2019, pp. 210-215.

44. M. A. Zaman and S. Katkoori, "Minimizing Performance and Energy Overheads Due to Fanout In Memristor based Logic Implementations," 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Verona, Italy, 2018, pp. 7-12.

45. L. K. Sah, S. A. Islam and S. Katkoori, "An Efficient Hardware-Oriented Runtime Approach for Stack-based Software Buffer Overflow Attacks," 2018 Asian Hardware Oriented Security and Trust Symposium (AsianHOST), Hong Kong, 2018, pp. 1-6. **Best Paper Candidate. 3 out of 19 full papers.**

46. S. A. Islam, L. K. Sah and S. Katkoori, "Empirical Word-Level Analysis of Arithmetic Module Architectures for Hardware Trojan Susceptibility," 2018 Asian Hardware Oriented Security and Trust Symposium (AsianHOST), Hong Kong, 2018, pp. 109-114.

47. S. A. Islam and S. Katkoori, "High-level synthesis of key based obfuscated RTL datapaths," 2018 19th International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, 2018, pp. 407-412.

48. L. Bozgeyikli, E. Bozgeyikli, A. Raij, R. Alqasemi, S. Katkoori, and R. Dubey, "Vocational Rehabilitation of Individuals with Autism Spectrum Disorder with Virtual Reality," *Proceedings of The 19th International ACM SIGACCESS Conference on Computers and Accessibility*, 2017.

49. L. Bozgeyikli, A. Raij, S. Katkoori, and R. Alqasemi, "Effects of Instruction Methods on User Experience in Virtual Reality Serious Games," *Proceedings of The 19th International Conference on Human-Computer Interaction*, 2017.

50. E. Bozgeyikli, A. Raij, S. Katkoori, and R. Dubey, "Point & Teleport Locomotion Technique for Virtual Reality," In Proceedings of the *2016 Annual ACM Symposium on Computer-Human Interaction in Play (CHI PLAY 2016)*, NY, USA, Pages(s): 205-216.

51. S. Aditham, N. Ranganathan, and S. Katkoori, "LSTM-Based Memory Profiling for Predicting Data Attacks in Distributed Big Data Systems," *2017 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW),* Orlando/Buena Vista, FL, USA, 2017, Page(s): 1259-1267.

52. E. Bozgeyikli, A. Raij, S. Katkoori, and R. Dubey, "Locomotion in Virtual Reality for Individuals with Autism Spectrum Disorder," In Proceedings of the *2016 ACM Symposium on Spatial User Interaction (SUI 16́)*, New York, NY, USA, Page(s): 33-42.

53. E. Bozgeyikli, L. Bozgeyikli, A. Raij, S. Katkoori, R. Alqasemi, and R. Dubey. "Virtual Reality Interaction Techniques for Individuals with Autism Spectrum Disorder: Design Considerations and Preliminary Results," In Proceedings, Part II, of the *18th International Conference on Human-Computer Interaction. Interaction Platforms and Techniques - Volume 9732, Masaaki Kurosu (Ed.), Vol. 9732. Springer-Verlag New York, Inc.,* New York, NY, USA, Page(s): 127-137.

54. L. Bozgeyikli, E. Bozgeyikli, A. Raij, R. Alqasemi, S. Katkoori, and R. Dubey, "Vocational Training with Immersive Virtual Reality for Individuals with Autism: Towards Better Design Practices," In *IEEE 2nd Workshop on Everyday Virtual Reality (WEVR)*, Greenville, SC, 2016, Page(s): 21-25.

55. L. Bozgeyikli, A. Raij, S. Katkoori, and R. Alqasemi, "Effects of Environmental Clutter and Motion on User Performance in Virtual Reality Game," In *Proceedings of ACM SIGCHI Annual Symposium on Computer-Human Interaction in Play (CHI PLAY) Workshop on Fictional Game Elements: Critical Perspectives on Gamification Design. CEUR Workshop Proceedings*, Vol-1715, 2016.

56. S. Aditham, N. Ranganathan and S. Katkoori, "Memory access pattern based insider threat detection in big data systems," *2016 IEEE International Conference on Big Data (Big Data)*, Washington, DC, 2016, Page(s): 3625-3628.

57. L. Bozgeyikli, A. Raij, S. Katkoori, and R. Alqasemi. "Effects of Visual Fidelity and View Zoom on Task Performance in Virtual Reality," In *Proceedings of The 13th Annual Conference of the European Association for Virtual Reality and Augmented Reality (EuroVR)*, November 2016.

58. O. Dokur, N. Elmehraz, and S. Katkoori, "Embedded System Design of a Real-time Parking Guidance System," *2016 Annual IEEE Systems Conference (SysCon)*, Orlando March 2016, Pages: 1-8.

59. S. Pendyala and S. Katkoori, "State Encoding based NBTI Optimization in Finite State Machines," *2016 International Symposium on Quality of Electronic Design (ISQED)*, March 2016, Page(s): 416-422.

60. R. P. O'Brien, S. Katkoori, M. A. Rowe, "Design and Implementation of an Embedded System for Monitoring At-home Solitary Alzheimerś Patients," *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2-5 Aug. 2015, Page(s):1-4.

61. S. Pendyala and S. Katkoori, "Self Similarity and Interval Arithmetic Based Leakage Optimization in RTL Datapaths," *2014 IEEE/IFIP 22nd International Conference on VLSI and System-on-Chip (VLSI-SoC)*, Oct. 2014. **Best Paper Candidate (5 best paper nominations. 31 full papers accepted out of 104 regular submission)**. *Invited for a Springer Book Chapter.*

62. M. Johnson, A. Fabregas, Z. Wang, S. Katkoori, and P-S. Lin, "Embedded System Design of an Advanced Illumination Measurement System for Highways," *8th Annual IEEE Systems Conference (SysCon)*, 2014, Page(s): 579 - 586.

63. N. Elmehraz, S. Katkoori, A. Kourtellis, and P-S. Lin, "Prototyping of a Portable Data Logging Embedded System for Naturalistic Motorcycle Study," *International Conference on Connected Vehicles and Expo (ICCVE)*, 2013. Page(s): 471 - 472.

64. C. Bell, M. Lewandowski, S. Katkoori, "A Multi-parameter Functional Side-channel Analysis Method for Hardware Trust Verification," *IEEE 31st VLSI Test Symposium (VTS)*, 2013, Page(s) 1-4.

65. I. Bahar, A. K. Jones, S. Katkoori, P. H. Madden, D. Marculescu, and I. L. Markov, "*Scaling* the impact of EDA education – Preliminary findings from the CCC workshop series on extreme scale design automation," *2013 IEEE International Conference on Microlectronic Systems Education (MSE)*, 2013, Page(s): 64-67.

66. C. S. Paidimarry, B. P. Kumar, and S. Katkoori, "A Novel Approach to Crosstalk Noise Analysis in CMOS Inverter driven Coupled RLC Interconnects," *2013 Annual IEEE India Conference (INDICON)*, 2013, Page(s): 1-6.

67. M. Lewandowski, R. Meana, M. Morrison, and S. Katkoori, "A Novel Method for Watermarking Sequential Circuits," *2012 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)*, June 2012, Page(s): 21-24.

68. S. Pendyala and S. Katkoori, "Interval arithmetic based input vector control for RTL subthreshold leakage minimization," *2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC)*, Oct. 2012, Page(s): 141-146.

69. S. Roy, N. Ranganathan, and S. Katkoori, "Compiler Directed Power Gating in Embedded Microprocessors," *IEEE International Conference on Computer Design (ICCD)*, October 2009, Page(s): 35-40.

70. S. Roy, N. Ranganathan, and S.Katkoori, "Exploration of Compiler Optimization Techniques for Enhancing Power Gating," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2009, Page(s): 1004-1007.

71. H. Sankaran and S. Katkoori, "Floorplan Driven High Level Synthesis for Crosstalk Noise Minimization in Macro-cell Based Designs," *IEEECS Annual Symposium on VLSI (ISVLSI)*, May 2009, Page(s): 274 - 279.

72. H. Sankaran and S. Katkoori, "On-chip Dynamic Worst-case Crosstalk Pattern Detection and Elimination for Bus-based Macro-cell Designs," *International Symposium on Quality Electronic Design (ISQED)*, March 2009, Page(s): 33 - 39.

73. V. Krishnan and S. Katkoori, "Simultaneous Peak Temperature and Average Power Minimization during Behavioral Synthesis," *22nd International Conference on VLSI Design (VLSID)*, January 2009, Page(s): 419 - 424.

74. S. Katkoori, P. Fernando, H. Sankaran, A. Stoica D. Keymeulen, and R. Zebulum, "Programmable Genetic Algorithm IP Core for Sensing and Surveillance Applications," *SPIE 2009 Conference*, 13-17th April 2009, Orlando.

75. H. Sankaran and S. Katkoori, "Simultaneous Scheduling, Allocation, Binding, Re-ordering, and Encoding for Crosstalk Pattern Minimization during High Level Synthesis," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, April 2008, Page(s): 423 - 428.

76. H. Sankaran and S. Katkoori, "Bus Binding, Re-ordering, and Encoding for Crosstalk-producing Switching Activity Minimization during High Level Synthesis," *4th IEEE Symposium on Electronic Design, Test, and Applications (DELTA)*, January 2008, Page(s): 454 - 457.

77. P. Fernando, H. Sankaran, S. Katkoori, D. Keymeulen, A. Stoica, R. Zebulum, R. Ramesham "A Customizable FPGA IP Core Implementation of a General-Purpose Genetic Algorithm Engine," *IEEE International Symposium on Parallel and Distributed Processing (IPDPS) 2008*, April 2008, Page(s): 1 - 8.

78. A. Mast, J. Montealegre, L. Jenkins, S. Katkoori, A. White, and C. Kimmery, "A High-Level Tool for Bit-level SEU Sensitivity Analysis in DSP Filters, *Military and Aerospace Applications of Progg. Devices and Technologies (MAPLD)*, September 2008, Baltimore, Maryland.

79. V. Krishnan and S. Katkoori, "A 3D-Layout Aware Binding Algorithm for High-Level Synthesis of Three-Dimensional Integrated Circuits," *8th International Symposium on Quality Electronic Design (ISQED)*, March 2007, Page(s): 885–892.

80. V. Krishnan and S. Katkoori, "Minimizing Wire Delays by Net-topology Aware Binding during Floorplan-driven High Level Synthesis," *2007 IFIP International Conference on Very Large Scale Integration (VLSI-SOC)*, October 2007, Page(s):99-104.

81. P. Fernando and S. Katkoori, "An Elitist Non-Dominated Sorting Based Genetic Algorithm for Simultaneous Area and Wirelength Minimization in VLSI Floorplanning," *21st International Conference on VLSI Design (VLSID)*, January 2008, Page(s): 337 - 342.

82. V. Krishnan and S. Katkoori "Clock Period Minimization with Iterative Binding Based on Stochastic Wirelength Estimation during High-Level Synthesis," *21st International Conference on VLSI Design (VLSID)*, January 2008, Page(s): 641 - 646.

83. A. Stoica, R. Zebulum, D. Keymeulen, R. Ramesham, J. Neff, and S. Katkoori, "Temperature-Adaptive Circuits on Reconfigurable Analog Arrays," *IEEE Aerospace Conference*, March 2007, Page(s): 1 - 6. (*No hardcopy proceedings.*)

84. D. Keymeulen, R. Zebulum, R. Rajeshuni, A. Stoica, S. Katkoori, S. Graves, F. Novak, and C. Antill, "Extreme Temperature Electronics based on Self-Adaptive System using Field Programmable Gate Array," *IEEE Aerospace Conference*, March 2007, Page(s):1 - 6. (*No hardcopy proceedings.*)

85. S. Katkoori, A. Stoica, D. Keymeulen, R. Zebulum, and R. Ramesham, Field Programmable Gate Arrays (FPGAs) in Extreme Environments - A Survey, *IMAPS 2nd Adv. Tech. Workshop on Reliability of Adv. Electronics in Extreme Cold Environments*, February 2007, Pasadena, CA.

86. W. Alvis, W.; S. Murthy, K. Valavanis, W. Moreno, M. Fields, and S. Katkoori, "FPGA based Flexible Autopilot Platform for Unmanned Systems," *2007 Mediterranean Conference on Control & Automation (MED)*, June, 2007, Page(s): 1 - 9.

87. S. Roy, S. Katkoori, and N. Ranganathan, "A Compiler Based Leakage Reduction Technique by Power-Gating Functional Units in Embedded Microprocessors," *20th International Conference on VLSI Design (VLSID)*, January 2007, Page(s): 215-220.

88. D. Keymeulen, R. Zebulum, R. Rajeshuni, A. Stoica, S. Katkoori, S. Graves, F. Novak, and C. Antill, "Self-Adaptive System Based on Field Programmable Gate Array for Extreme Temperature Electronics," *First NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, June 2006 Page(s):296 - 300.

89. A. Stoica, R. S. Zebulum, D. Keymeulen, R. Ramesham, J. Neff, and S. Katkoori, "Temperature-Adaptive Circuits on Reconfigurable Analog Arrays," *First NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, June 2006 Page(s):28 - 31.

90. V. Krishnan and S. Katkoori, "Design Space Exploration of RTL Datapaths using Rent Parameter based Stochastic Wirelength Estimation," *7th International Symposium on Quality Electronic Design (ISQED)*, March 2006, Page(s): 363 - 369.

91. R. Gopalan, C. Gopalakrishnan, and S. Katkoori, "Leakage Power Driven Behavioral Synthesis of Pipelined Datapaths," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 2005, Page(s):167 - 172.

92. H. Sankaran, S. Katkoori, and U. Kailasam, "System Level Energy Optimization for Location-Aware Computing," *IEEE Conference on Pervasive Computing (PerCom)*, March 2005, Page(s): 319 - 323.

93. H. Li, S. Katkoori, and Z. Liu, "Feedback Driven High Level Synthesis for Performance Optimization," *6th International Conference On ASIC (ASICON)*, Volume 2, October 2005, Page(s): 961 - 964.

94. S. Kakarla and S. Katkoori, "Partial Evaluation Based Redundancy for SEU Mitigation in Combinational Circuits," *Military and Aerospace Applications of Progg. Devices and Technologies (MAPLD)*, September 2005.

95. H. Li, S. Katkoori, and W-K. Mak, "Force-Directed Performance Driven Placement Algorithm for FPGAs," Proceedings of *IEEE Computer society Annual Symposium on VLSI (ISVLSI)*, February 2004, Page(s):193 - 198.

96. C. Gopalakrishnan and S. Katkoori, "Tabu Search Based Behavioral Synthesis of Low Leakage Datapaths," *IEEE Computer society Annual Symposium on VLSI (ISVLSI)*, February 2004, Page(s): 260 - 261.

97. S. Gupta and S. Katkoori, "A Fast Word-Level Estimation Technique for Intra-Crosstalk," *Design, Automation and Test in Europe (DATE) Conference*, Volume 2, February 2004, Page(s): 1110-1115.

98. S. Alupoaei and S. Katkoori, "Energy Model Based Macrocell Placement for Wirelength Minimization," Proceedings of *17th International Conference on VLSI Design (VLSID)*, January 2004, Page(s): 713 - 716.

99. S. Alupoaei and S. Katkoori, "Ant Colony Optimization Technique for Macrocell Overlap Removal," Proceedings of *17th International Conference on VLSI Design (VLSID)*, January 2004, Page(s): 963 - 968.

100. S. Gupta and S. Katkoori, "Intra-Bus Crosstalk Estimation Using Word-Level Statistics," Proceedings of *17th International Conference on VLSI Design (VLSID)*, January 2004, Page(s): 449 - 454.

101. C. Gopalakrishnan and S. Katkoori, "KnapBind: An Area-Efficient Binding Algorithm for Low-leakage Datapaths," Proceedings of *21st International Conference on Computer Design (ICCD)*, October 2003, Page(s): 430 - 435.

102. P. Samudrala, J. Ramos, and S. Katkoori, "Selective Triple Modular Redundancy for SEU Mitigation in FPGAs," *Military and Aerospace Applications of Progg. Devices and Technologies (MAPLD)*, September 2003.

103. C. Gopalakrishnan and S. Katkoori, "A Fast Hierarchical Leakage Power Simulator for VHDL Structural Descriptions," *IEEE Computer Society Symposium on VLSI (ISVLSI)*, February 2003, Page(s): 211-212.

104. H. Li, W. K. Mak, and S. Katkoori, "An Efficient LUT-Based FPGA Technology Mapping Algorithm for Power Minimization," *Asia-Pacific Design Automation Conference (ASPDAC)*, January 2003, Page(s): 353-358. **Nominated for Best Paper Award.**

105. C. Gopalakrishnan and S. Katkoori, "Resource Allocation and Binding for Low Leakage Power," *16th International Conference on VLSI Design (VLSID)*, January 2003, Page(s): 297-302.

106. C. Gopalakrishnan and S. Katkoori, "Behavioral Synthesis of Datapaths with Low Leakage Power," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Volume: 4, May 2002, Page(s): 699 -702.

107. S. Gupta and S. Katkoori, "Force-directed Scheduling for Dynamic Power Optimization," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, April 2002, Page(s): 68-73.

108. C. Gopalakrishnan and S. Katkoori, "Power Optimization using Input Transformations," *First IEEE Intl. Workshop on Electronic Design, Test, & Applications (DELTA)*, January 2002, Page(s): 154-158.

109. S. Alupoaei and S. Katkoori, "Net Clustering Based Macro-cell Placement," *15th International Conference on VLSI Design (VLSID)*, January 2002, Page(s): 399-404.

110. H. Li, W. K. Mak, S. Katkoori, "Low Power Mapping for FPGAs with Optimal Depth," *IEEE Computer Society Workshop on VLSI (WVLSI)*, April 2001, Page(s): 123-128.

111. S. Katkoori and S. Alupoaei, "RT-level Interconnect Optimization in DSM Regime," *IEEE Computer Society Workshop on VLSI (WVLSI)*, April 2000, Page(s): 143-148.

112. S. Katkoori and R. Vemuri, "Scheduling for Low Power under Resource and Latency Constraints," *International Symposium on Circuits and Systems (ISCAS)*, May 2000, Vol. 2, Page(s): 53-56.

113. A. Durbha and S. Katkoori, "Route-and-Place Design Methodology for Interconnect Optimization in DSM Regime," *X IFIP International Conference on Very Large Scale Integration (IFIP VLSI)*, December 1999, Page(s): 427-438.

114. P. Maurer, S. Katkoori, W. Mak, M. Varanasi, "Component-Level Programming: A Revolution in Software Technology," Proceedings of the Frontiers in Education Conference, Proceedings of the *29th Annual Frontiers in Education Conference*, Volume 2, November 1999, Page(s): 12B1/11 -12B1/15.

115. S. Katkoori and R. Vemuri, "Accurate Resource Estimation Algorithms for Behavioral Synthesis," *Great Lakes Symposium on VLSI Conference (GLSVLSI)*, March 1999, Page(s): 338-339.

116. V. Natesan, A. Gupta, S. Katkoori, D. Bhatia, and R. Vemuri, "A Constructive Method for Data Path Area Estimation During High-Level VLSI Synthesis," *Asia and South-Pacific Design Automation Conference (ASPDAC)*, January 1997, Page(s): 509 - 515.

117. S. Katkoori and R. Vemuri, "Simulation Based Architectural Power Estimation for PLA-Based Controllers," *International Symposium on Low Power and Electronic Design (ISLPED)*, August 1996, Page(s): 121-124.

118. S. Katkoori, J. Roy, and R. Vemuri, "A Hierarchical Register Optimization Algorithm for Behavioral Synthesis," *9th International Conference on VLSI Design (VLSID)*, January 1996, Page(s): 126-134.

119. S. Katkoori and R. Vemuri, "A Power Simulator for VHDL Structural Descriptions," *VHDL International User's Forum (VIUF) Fall Conference,* October 1995, Page(s): 4.17-4.25.

120. S. Katkoori, N. Kumar and R. Vemuri, "High Level Profiling Based Low Power Synthesis Technique," *International Conference on Computer Design (ICCD)*, October 1995, Page(s): 446-452.

121. S. Katkoori, N. Kumar, L. Rader and R. Vemuri, "A Profile Driven Approach for Low Power Synthesis," *IFIP Intl. Conference on VLSI Design (VLSID)*, August 1995, Page(s): 759-765.

122. D. Bhatia, R. Rajagopalan, and S. Katkoori, "Hierarchical Reconfiguration of VLSI/WSI Arrays," *7th International Conference on VLSI Design (VLSID)*, January 1994, Page(s): 349-352.

ADMINISTRATIVE SERVICES TO UNIVERSITY

- Chair, CSE Graduate Committee, May 2014 – May 2016.
- Graduate Program Director, Computer Science & Engineering, May 2014 – May 2016.
- Member, USF Tampa Technology Fee Advisory Council, 2010-2012.
- Member, USF CoE Dean Search Committee, 2014.
- Chair, USF CoE Outstanding Undergraduate Teaching Award Committee, 2010-2011.
- CSE Department Representative, USF CoE Faculty Governance Committee, 2011-2014.
- CoE Senator, USF Senate, 2010-2016 (two terms).
- CoE Representative, USF Council on Educational Policies and Issues, 2010-2013.
- CoE Representative, USF Honors and Awards Council, 2010-2013.
- Member, CSE Graduate Committee, 2009-2010.
- Member, Planning & External Relations Committee, 2009-2010.
- Departmental representative, Inaugural CoE Eminent Lecture Series, Spring 2009.
- Graduate Program Director, Computer Science & Engineering, May 2006–April 2009.
- Departmental Co-ordinator, Alfred P. Sloan Program, CoE, USF, May 2006–Dec 2008.
- College Grievance Committee, Summer 2006 (Chair), Spring 2009 (Member).
- Departmental Tenure & Promotion Committee, 2004–present.
- Graduate Admissions Co-ordinator, 2004–2005.
- Member, Graduate Admissions Committee, 2003–2009.
- Member, Departmental Infrastructure Committee, 2003–2009.
- Supervisor for the Departmental Technical Support 1999–2003.
- Departmental representative on the Safety and Health Committee 2000–present.
- Departmental representative on the interdepartmental committee on Packaging 1998-99.
- Departmental library representative 1998–2001.
- 1998/99 Departmental representative to Graduation.
- MS Comprehensive and PhD Qualifiers Examination Committee, Computer Architecture Section (Fall & Spring Semesters, 1997–present).
- MS Comprehensive and PhD Qualifiers Examination Committee, Member of the sub-committee on the Advanced Digital Systems (ADS)(Fall 1998, Spring 1999).
- On the undergraduate curriculum evaluation committee for planning, development, and evaluation of computer engineering program (Fall 1997).

SERVICE TO PROFESSION

Journals

- Associate Editor, IEEE Transactions on Consumer Electronics, Feb 2022 – current.
- Associate Editor, IEEE Consumer Electronics Magazine, Jan 2021 – current.
- Associate Editor, IEEE Embedded Systems Letters, July 2020 – current.
- Associate Editor, Springer Nature Computer Science (Emerging Trends in Sensors, IoT, and Smart Systems), Feb 2020 – current.
- Associate Editor, IEEE Transactions on VLSI Systems, Nov 2006 - Dec 2009.
- Reviewer, IEEE Access, 2014.
- Reviewer, IEEE Transactions on Computer-Aided Design of ICs and Systems.
- Reviewer, IEEE Transactions on Computers.
- Reviewer, IEEE Transactions on Evolutionary Computation.

- Reviewer, IEEE Transactions on VLSI Systems.
- Reviewer, ACM Transactions on Design Automation of Electronic Systems (TODAES).
- Reviewer, Journal on Low Power Electronics (JOLPE).
- Reviewer, Journal of Intelligent and Robotic Systems.
- Reviewer, Journal on VLSI Signal Processing Systems.
- Reviewer, Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3).
- Reviewer, IEE Proceedings on Computers & Digital Techniques.
- Reviewer, The Computer Journal.
- Reviewer, Integration, the VLSI Journal.

Conferences, Symposia, and Workshops

General Chair

- General Co-Chair, 2022 International Symposium on Smart Electronics Systems, 19-21, December 2022
- General Co-Chair, 5th IFIP International Internet-of-Things (IoT) Conference, Amsterdam, NL 27-28 October 2022.
- General Co-Chair, 2nd IFIP International Internet-of-Things (IoT) Conference, Tampa, FL, 31st October - 1st November 2019.
- General Co-Chair, 5th IEEE International Symposium on Smart Electronic Systems (iSES), Rourkela, India, 16-18th, December 2019.
- General Co-Chair, ACM Student Research Competition at Design Automation Conference (DAC), 2011
- General Co-Chair, ACM Student Research Competition at ICCAD, 2014.
- General Co-Chair, 2001 IEEECS Workshop on VLSI, Orlando, FL.

Program Chair

- Program Co-Chair, Great Lakes Symposium on VLSI (GLSVLSI) 2023, Knoxville, 5-7 June 2023.
- Program Co-Chair, 4th IFIP International Internet-of-Things (IoT) Conference, Amsterdam, NL, 4 - 5 November, 2021.
- Program Co-Chair, International Symposium on VLSI (ISVLSI), Tampa, FL, 2021.
- Program Co-Chair, 39th International Conference on Consumer Electronics (ICCE), 10-12 January 2021.
- Program Co-Chair, 3rd IFIP International Internet-of-Things (IoT) Virtual Conference, Tampa, FL, 5 - 6 November, 2020.
- Co-organized Workshop with Dr. Meredeth Rowe at 2015 Aging in America, 23- 27 March, Chicago, entitled, "Envisioning Smart Support System for Working Caregivers of Patients with Dementia – Smart Support Technologies."
- Co-organized "Workshops on Extreme Scale Design Automation (ESDA) – Challenges and Opportunities for 2025 and Beyond," with R. I. Bahar, A. K. Jones, S. Katkoori, P. H. Madden, D. Marculescu, and I. L. Markov. CCC funded effort to layout the vision for EDA field for next 10-25 years.
  Final Report: http://www.cra.org/ccc/files/docs/esda/CCC_ESDA%20Report.pdf

Registration, Publicity, Local Arrangements Chair

- Registration & Publicity Chair, 2000 IEEECS Workshop on VLSI, Orlando, FL
- Local Arrangements Chair, 2009 Intl. Symposium VLSI 2009, Tampa, FL

Session Chair

- Session Chair, IMAPS 2007 Workshop on Extreme Cold Electronics.
- Session Chair, "Synthesis," 1999 Great Lakes Symposium on VLSI (GLSVLSI).
- Session Chair, "Low Power Design," 2008 International Conference on VLSI Design.

Track Co-Chair

- Track Co-Chair, Design Automation & CAD tools Track, 17th International Conference on Embedded Systems & 31st International Conference on VLSI Design
- Track Co-Chair, Great Lakes Symposium on VLSI 2017
- Track Co-Chair, Digital Circuits and Systems, MWSCAS 2017
- Track Co-Chair, EDA Track, ISQED 2017
- Track Co-Chair, VLSI Track, GLSVLSI 2016
- Track Co-Chair, EDA Track, ISQED 2015
- Track Co-Chair, EDA Track, ISQED 2013
- Track Co-Chair, Security Track, IFIP VLSI-SOC 2015
- Forum Co-Chair, PhD Forum, IFIP VLSI-SOC 2015

TPC Member

- TPC Member, CASES, Embedded Systems Week, 2018
- TPC Member, IFIP VLSI System-on-a-Chip (SOC) Conference, 2017
- TPC Member, Intl. Symposium on Quality of Electronic Design (ISQED) 2006, 2008
- TPC Member, IEEE Computer Society Symposium on VLSI (ISVLSI)
- TPC Member, Intl. Conference on Computer Design (ICCD), 2017
- TPC Member, Intl. Conference on Computer Design (ICCD), 2005
- TPC Member, Reconfigurable Architectures Workshop (RAW), (Years: 2005, 2008)
- TPC Member, Field Programmable Logic (FPL), 2008,
- TPC Member, IFIP VLSI System-on-a-Chip (SOC) Conference
- TPC Member, Asian Symposium on Quality of Electronic Design (ASQED)
- TPC Member, IEEE SOC Conference, Portland, OR, 2003

Reviewer

- Reviewer, ACM Student Research Competition Finals, 2017
- Reviewer, Intl. Symposium on Quality of Electronic Design (ISQED), 2015
- Reviewer, Design Automation Conference (DAC), 2014
- Reviewer, Micro-electronics System Education (MSE), 2007
- Reviewer, Design Automation Conference (DAC), 2008
- Reviewer, Military and Aerospace Programmable Logic Devices (MAPLD), 2005
- Reviewer, Intl. Syposium on Circuit and Systems (ISCAS)

- Reviewer, Midwest Symposium on Circuit and Systems (MWSCAS) 2008
- Reviewer, Intl. Conf. on Embedded Software and Systems (ICESS) 2007
- Reviewer, Intl. Conf. on VLSI Design, 2008
- Reviewer, IEEE System on a Chip (SOC) Conference
- Reviewer, Adaptive Hardware Systems AHS 2006
- Reviewer, NSF SBIR Panel, 2003.
- Reviewer, DAC PhD Forum, 2004
- Reviewer, International Conference on Computer Design (ICCD), 2004

Other Service

- Faculty Advisor, USF HKN Group, Fall 2011 - Fall 2014.
- Faculty Advisor, USF YES+ Group, Spring 2014-present.
- Faculty Advisor, USF IEEE Computer Society Student Chapter, Fall 2017-Fall 2020.
- Lecturer, 2011 ACM SIGDA Design Automation Summer School (DASS).
- Treasurer, ACM SIGDA, Fall 2010 – Summer 2012.
- Board Member, ACM SIGDA Fall 2010 – Summer 2012.
- Publicity Chair and Organizing Member, ACM Cadathlon Contest, Nov. 2009.
- IEEE Senior Member Review Panel, Tampa, FL, Spring 2009.
- Judge, USF Research Day, Engineering Research Poster Contest, Spring 2009.
- Mentor, Undergraduate Research Competition, Spring 2008.
- Editor-in-Chief, *The Suncoast Signal*, IEEE Florida West Coast Section (FWCS) Monthly Newsletter,
- Judge, USF EE Senior Project Poster Competition, Fall 2006.
- Faculty Advisor, USF IEEE Computer Society Student Chapter 1999-2005.
- Mentor, Research Experiences for Teachers (RET), Summer 2004.
- Proposal Reviewer, Florida I4 High Tech Corridor Grant Program, Summer 2004.

GRADUATE THESIS/DISSERTATION COMMITTEES

PhD Dissertation Committee Member

At USF

1. Shakil Mahmud, "*Enhancing Safety and Reliability of Closed-loop Medical Control Systems*," Advisor: Dr. Robert Karam, CSE Dept., Summer 2023.
2. Aldin Vehabovic, "*Machine Learning Approach for Static Ransomware Analysis*," Advisor: Dr. Nasir Ghani, EE Dept., Summer 2023
3. Jasmin Kaur, "*Secure Lightweight Cryptographic Hardware Constructions for Deeply Embedded Systems*," Advisor: Dr. Mehran Mozzaffari Kermani, CSE Dept., Summer 2023.
4. Hye Seon Yi, "*Automated Approaches to Enable Innovative Civic Applications from Citizen Generated Imagery*," Advisor: Dr. Sriram Chellappan, CSE Dept., Spring 2023.
5. Brooks Olney, "*From Hardware to Software: Defending the Next Generation of AI and ML Applications*," Advisor: Dr. Robert Karam, CSE Dept., Spring 2023.
6. Sylwester Sobolewski, "*Recognition of Modern Modulated Waveforms with Applications to ABMS and VDATS Test Program Set Development*," Advisor: Dr. Ravi Sankar, EE Dept., Fall 2022.

7. Arup Kanti Dey, "*Design, Deployment, and Validation of Computer Vision Techniques for Societal Scale Applications*," Advisor: Dr. Sriram Chellappan, CSE Dept., Summer 2021.
8. Chetana Murudkar (Advisor: Dr. Rich Gitlin, EE, USF), Fall 2019 –TBD.
9. Yuting Cao (Advisor: Dr. Hao Zheng, CSE, USF), Fall 2019.
10. Tony Casagrande (Advisor: Dr. N. Ranganathan, CSE, USF), 2014
11. Ravi Panchumurthy (Advisor: Dr. S. Sarkar, CSE, USF), 2014
12. Danielle Ferguson (Advisor: Dr. J. Ligatti, CSE, USF)
13. Murat Karabacak (Advisor: Dr. H. Arslan, EE USF)
14. Himanshu Thapliyal (Advisor: Dr. N. Ranganathan, CSE, USF)
15. Matt Morrison (Advisor: Dr. N. Ranganathan, CSE, USF)
16. Saurabh Kotiyal (Advisor: Dr. N. Ranganathan, CSE, USF)
17. Mehrgan Mostowfi (Advisor: Dr. K. Christensen, CSE, USF)
18. Yue Wang (Advisor: Dr. N. Ranganathan, CSE, USF)
19. Sylwester N. Sobolewski, (Advisor: Dr. R. Sankar, EE, USF)
20. Chao He (Advisor: Dr. R. Gitlin, EE, USF)
21. David Aguilar (Advisor: Dr. Rafael Perez), Fall 2007
22. Saraju Mohanty (Advisor: Dr. N. Ranganathan, CSE, USF), Fall 2003
23. Thara Rejimon (Advisor: Dr. Sanjuktha Bhanja, EE, USF),
24. Sanjukta Bhanja (Advisor: Dr. N. Ranganathan, CSE, USF), Fall 2002
25. Mahalingam Venkataraman (Advisor: Dr. N. Ranganathan, CSE, USF), Spring 2009
26. Koustav Bhattacharya (Advisor: Dr. N. Ranganathan, CSE, USF), Fall 2009
27. Ashok Murugavel (Advisor: Dr. N. Ranganathan, CSE, USF), Spring 2003
28. Upavan Gupta (Advisor: Dr. N. Ranganathan, CSE, USF), Summer 2008
29. Alberto Rodriguez (Advisor: Dr. Tom Weller, EE, USF)
30. Jorge Galvis (Advisor: Dr. Wilfredo Moreno, EE, USF)
31. Madhusmita Behera, Moffitt Cancer Center (Advisor: Dr. John Hines), USF

Outside USF

1. Jawad Khan, ECECS, Univ. of Cincinnati (Advisor: Dr. Ranga Vemuri)
2. Xin Jia, ECECS, Univ. of Cincinnati (Advisor: Dr. Ranga Vemuri)
3. Shubhankar Basu (Advisor: Dr. Ranga Vemuri, ECECS, Univ. of Cincinnati), Spring 2008
4. Madhubanthi Mukherjee, ECECS, Univ. of Cincinnati (Advisor: Dr. Ranga Vemuri)
5. Manish Handa, (Advisor: Dr. Ranga Vemuri, ECECS, Univ. of Cincinnati),
6. Preetham Lakshmikanthan (Advisor: Dr. Adrian Nunez, ECE, Syracuse University)

MS Thesis Committee Member

1. Dmytro Vitel, CSE (Advisor: Dr. Alessio Gaspar), Fall 2019.
2. Brian Hayes, CSE (Advisor: Dr. Ranganathan),
3. Vasanth Ramesh, CSE (Advisor: Dr. Ranganathan),
4. Ryan Mabry (Advisor(s): Dr. N. Ranganathan and Dr. H. Zheng) Defended in Summer 2007.
5. Shankar Arumuguvelu (Advisor: Dr. N. Ranganathan) Defended in Summer 2007.
6. Alejandro G. Munoz (Advisor(s): Dr. Larry Hall and Dr. D. Goldgof), Fall 2008.
7. Zornitza Genova (Advisor: Dr. Martha Escobar Moleno)
8. Arun Solleti (Advisor: Dr. Ken Christensen)

9. Jared Ahrens, (Advisor: Dr. Hao Zheng)
10. Khalid N. Hamzan, (Advisor: Dr. Peter Maurer)
11. Rohini K. Jella, (Advisor: Dr. Dewey Rundus)
12. Praveen Ikkurthy (Advisor: Dr. Miguel Labrador)
13. Subodh Kerkar (Advisor: Dr. Miguel Labrador)
14. Vipul Mistry (Advisor: Dr. Murali Varanasi)
15. Sunil Chappidi (Advisor: Dr. N. Ranganathan)
16. Sivakumar Bakthavachalu (Advisor: Dr. Miguel Labrador)
17. Alejandro G. Munoz (Advisor: Dr. Larry Hall)
18. Joshua Johnson (Advisor: Dr. Eugene Fink)
19. Srinath Chavali (Advisor: Dr. N. Ranganathan)
20. Mohammed Gharawi (Advisor: Dr. Peter Maurer)
21. Karthikeyan Balakrishnan (Advisor: Dr. N. Ranganathan)
22. Yiting Cao (Advisor: Dr. H. Zheng, CSE, USF)
23. Anurag Panwar (Advisor: Dr. S. Chellapan, CSE, USF)
24. Michael Nachtigal (Advisor: Dr. N. Ranganathan, CSE, USF)

PhD Dissertation Defense Chair

At University of South Florida, the Graduate School requires the PhD defense to be chaired by a Professor outside the candidate's department.

1. Bhaskar Tetali, EE (Advisor: Dr. Chris Ferrikides), Spring 2005
2. Balaji Lakshminarayanan, EE (Advisor: Dr. Tom Weller), Fall 2005
3. Charles Baylis (Advisor(s): Dr. Larry Dunleavy and Dr. Dave Snider, EE, USF), Spring 2007
4. Son Ho (Advisor: Dr. Muhammad Rahman, MechE, USF), Summer 2007
5. Saravana Natarajan (Advisor: Dr. Tom Weller, EE, USF), Fall 2007
6. Sathyaharish Jeedigunta, EE, USF (Advisor(s): Dr. Ashok Kumar, MechE, and Dr. Shekhar Bansali, EE), Spring 2008
7. Subramanian Krishnan, EE, USF (Advisors: Dr. Shekhar Bhansali, EE, and Dr. Lee Stefanakos, EE), Spring 2008
8. Carlos L. Castillo (Advisors: Dr. Wilfredo Moreno, EE, and Dr. Kimon Valavanis, CSE), Spring 2008
