# THE GENERALIZED DISCONTINUOUS PWM MODULATION SCHEME FOR THREE-PHASE VOLTAGE SOURCE INVERTERS

**Olorunfemi Ojo, and Parag Kshirsagar**
Department of Electrical and Computer Engineering
Laboratory for Electric Machines and Power Electronics/Center for Electric Power
Tennessee Technological University, Cookeville, TN 38505, USA
Phone : (931)-372-3869, Fax : (931)-372-3436, E-mail : jojo@tntech.edu

**Abstract :** This paper presents analytical techniques for the determination of the expressions for the modulation signals used in the carrier-based non-sinusoidal and generalized discontinuous PWM modulation (GDPWM) schemes for two-level, three-phase voltage source inverters. The resulting modulation schemes are applicable to inverters generating balanced or unbalanced phase voltages feeding either star or delta connected loads. The results presented in this paper analytically generalize the several expressions for the modulation signals already reported in the literature. Confirmatory experimental results are provided to illustrate some of the feasible modulation signals.

## I. INTRODUCTION

Three phase DC/AC Voltage Source Inverters (VSI's) schematically shown in Figure 1 (a) are now used extensively in motor drives, active filters and unified power flow controllers in power systems and uninterrupted power supplies to generate controllable frequency and AC voltage magnitudes using various pulse-width modulation (PWM) strategies. Of the possible PWM methods, the carrier-based PWM is very popular due to its simplicity of implementation, defined harmonic waveform characteristics and low harmonic distortion. Two main implementation techniques exist for PWM: the direct digital method and the sine-triangle intersection scheme. In the traditional sine-triangle intersection PWM (SPWM) technique, three reference modulation signals are compared with a triangular carrier signal and the intersections define the switching instants of the controllable devices [1]. It has been shown that the properties of the three-phase voltage source inverters feeding three-phase star-connected loads can be improved by augmenting the modulation signals with an appropriate zero sequence or non-sinusoidal waveform. The absence of a neutral wire in star-connected three-phase loads provides this degree of freedom in modulation methodology since the voltage between the neutral of the load and the reference of the DC source, $V_{pn}$ can take any value. This zero sequence waveform is used to alter the duty cycle of the inverter switches. Adding the same zero sequence waveform to each of the three reference phase voltages does not change the inverter output line-line voltage per carrier cycle average value; however, if the waveform is properly selected, one can achieve any of the followings: switching losses can be drastically reduced, the waveform quality may be improved, the linear modulation range can be extended, and common mode voltage of motor drives can also be drastically diminished. These potentials have been explored leading to investigations into and determination of various zero sequence waveforms, resulting in a large number of published carrier-based PWM methods [2-6 and references therein]. When the augmenting zero sequence waveform is continuous, the continuous PWM (CPWM) scheme is produced; however when the zero sequence signal is discontinuous with a potential for the modulator to have phase segments clamped either to the positive or negative rails, the scheme is called the discontinuous PWM (DPWM). The non-sinusoidal PWM may operate either as a CPWM or DPWM. A distinction between CPWM and DPWM has been clarified in [2]. In the CPWM methods, the modulation signals are always within the triangle peak boundaries and since the carrier and modulation signals intersect every carrier cycle, the devices are always turning on and off. On the other hand, in most DPWM schemes, the modulation signal of a phase has at least one segment which is clamped to either the positive or negative rail for at most a total of 120 degrees. A carrier-based PWM scheme with a generalized phase-shift dependent discontinuous modulation waveforms which captures all of the known discontinuous modulation signals has been discovered and coined the Generalized Discontinuous PWM (GDPWM). [2-3]

A three-phase DC/AC inverter has eight possible switching states producing distinct eight load line to inverter reference voltages; which when transformed to the stationary reference frame, the qd voltages can be displayed on a complex plane shown in Figure 1(b). The zero sequence voltages for all the switching states are shown in the figure for completeness. There are six active vectors (having non-zero qd voltages) and two null (zero) vectors in which the qd voltages are zero. In the direct digital PWM method, the complex plane qd output voltage vector of the three-phase voltage source inverter in the stationary reference frame is used to calculate the turn-on times of the inverter switching devices required to synthesize a reference three-phase balanced voltage set. In general, the three-phase balanced voltages expressed in the stationary reference frame; situated in the appropriate sector in Figure 1(b) are approximated by the time-average over a sampling period (converter switching period) of two adjacent active qd voltage inverter vectors and two zero states $U_0$ and $U_7$. The switching turn-on times of the two active and two null states are utilized to determine the duty cycle information to program the active switch gate signals [7].
The degree of freedom occasioned by the non-connection of the star point of the three-phase loads appears as the

partitioning of the total time the devices in the two zero states are utilized [3]. It has been conclusively shown that changing the ratio by which the two zero states are applied in the direct digital implementation produces the same effect on the inverter performance as the classical sine-triangle intersection technique in which the modulation signals are augmented with an appropriate zero sequence signal [7-9]. It therefore follows that the same AC voltages with similar characteristics can be synthesized by either of the two techniques. Due to the simplicity of the sine-triangle algorithm, analog or digital/microprocessor implementation is presumed to be easier to develop when compared to the direct digital implementation, which is more intense both from computational and complexity view points [5,8].

A study of the Generalized Discontinuous PWM (GDPWM) algorithm for three-phase inverters feeding a star-connected load and based on the "magnitude tests" has been confirmed with experimental results. Its advantages over the traditional sine-triangle PWM (without zero sequence waveform) in terms of improved waveform quality, lower switching losses, extended linear modulation range and increased voltage gain especially at high modulation index [2-3] have been demonstrated. Inspired by the seminal contributions in [2-3,9] on three-phase inverters feeding star-connected loads, this paper sets forth an approach to develop a comprehensive methodology for the determination of the non-sinusoidal and Generalized Discontinuous PWM modulation signals which are succinctly expressed in terms of the reference three-phase voltages which may be balanced or unbalanced and feeding either star or delta connected loads. In the first case, an expression for the generalized/non-sinusoidal zero sequence voltage waveform is determined based on the average of the zero sequence voltages of the two active and two null vector of the space vector. This result is similar to the zero sequence expression given in [10-11]. Our second significant contribution is the development of the expressions for the discontinuous modulating signals for the switching devices of the voltage source inverter connected to either star or delta connected loads. This scheme is also called a Generalized Discontinuous PWM in that the modulation signals of the six devices are inherently discontinuous, which with a variation of a parameter representing the zero state partitioning within the expression for the modulation signals yield an infinite number of modulation possibilities. It will be shown presently that when the zero partitioning parameter is either zero or unity and for any depth of modulation magnitude, each switch ceases to switch for a total of 120 degrees per fundamental cycle. Under this condition, the switching losses and effective converter switching frequency are significantly reduced. Furthermore, it is shown that with the zero partitioning parameter defined in a certain form, the non-sinusoidal and discontinuous modulation schemes yield the same waveform; affirming their sameness. When the desired three-phase voltages are unbalanced, expressions for modulation signals for CPWM and GDPWM are developed. This aspect of the paper is considered novel.

This paper has a strong educational value in that the modulation techniques are derived in a transparent and easy-to- understand fashion in the process of which the equivalence of the techniques of the carrier-based and direct digital PWM techniques are established. Significantly, the methodology for arriving at the expressions for the discontinuous modulation signals for the three-phase inverter can be extended for the determination of the discontinuous modulation signals for four-leg DC/AC inverters, three-phase DC/AC current source converters and various types of multi-level and minimalist converters feeding either delta or star-connected loads. The proposed carrier-based non-sinusoidal and discontinuous modulation schemes are experimentally implemented with an Analog ADMC401 DSP and used to modulate a three-phase inverter feeding a three-phase induction machine. Experimental waveforms are shown to justify the theory for the determination of the Generalized Discontinuous Modulation for three-phase, two-level converters.

## II. SPACE VECTOR MODULATION

The turn-on and turn-off sequences of any of the switching transistors of the three-phase voltage source inverter shown in Figure 1(a) are represented by an existence function which has a value of unity when it is turned on and becomes zero when it is turned off. In general, an existence function of a two-level converter is represented by $\mathbf{S_{ij}}$ , i = a,b,c, and j = p, n, where i represents the load phase to which the device is connected, and j signifies top (p) and bottom (n) device of an inverter leg. Hence $\mathbf{S_{ap}}$, $\mathbf{S_{an}}$ which take values of zero or unity, are respectively the existence functions of the top device ($\mathbf{T_{ap}}$) and bottom device ($\mathbf{T_{an}}$) of the inverter leg which are connected to phase 'a' load [12]. The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input DC voltage $V_d$ are given as :

$$0.5V_d\,(S_{ap} - S_{an}) = V_{ap} + V_{pn}$$

$$0.5V_d\,(S_{bp} - S_{bn}) = V_{bp} + V_{pn}$$

$$0.5V_d\,(S_{cp} - S_{cn}) = V_{cp} + V_{pn} \qquad (1)$$

In equations in (1), $V_{ap}$, $V_{bp,}$ $V_{cp}$ are the phase voltages of the load while the voltage of the load neutral to inverter reference is $V_{pn}$. If the reference voltage set is balanced, the load voltages from (1) are expressed in (2). The eight feasible switching modes for the three-phase voltage source inverter are enumerated in Table 1.

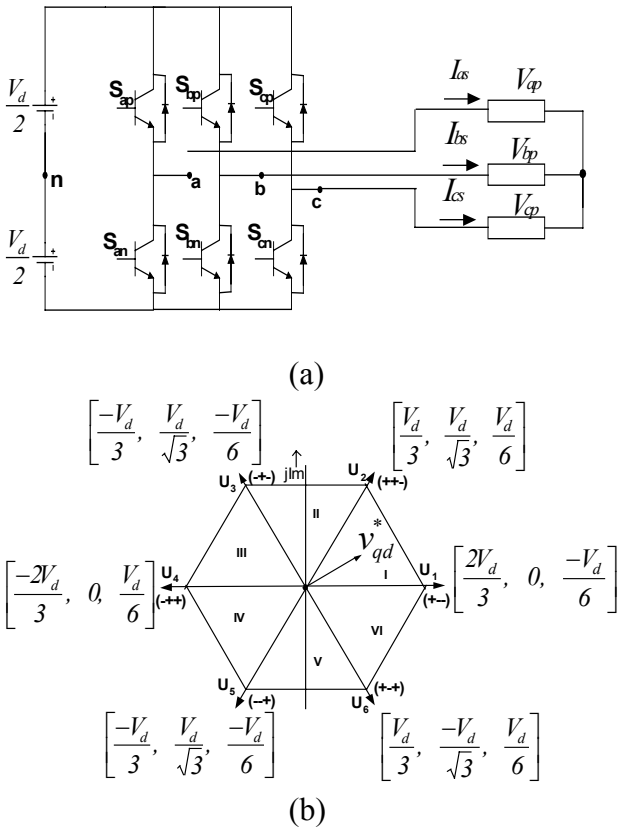



Figure 1: 2-Level PWM Voltage Source Inverters . (a) Three-phase with six switching devices, (b) Voltage space vector diagram including zero sequence voltages

$$V_{ap} = V_d(2S_{ap} - S_{bp} - S_{cp} - 2S_{an} + S_{bn} + S_{cn})/6$$

$$V_{bp} = V_d(-S_{ap} + 2S_{bp} - S_{cp} + S_{an} - 2S_{bn} + S_{cn})/6 \qquad (2)$$

$$V_{cp} = V_d(-S_{ap} - S_{bp} + 2S_{cp} + S_{an} + S_{bn} - 2S_{cn})/6$$

The stationary reference frame qdo voltages of the switching modes, also given in Table 1, are expressed in the complex variable form as ( $a = e^{j\varsigma}$, $\varsigma = 120°$) :

$$V_{qds} = 2/3(V_{ap} + a\,V_{bp} + a^2\,V_{cp})$$

$$V_o = 1/3(V_{ap} + V_{bp} + V_{cp}) \qquad (3)$$

$$V_{qs} = 1/6(2S_{ap} - S_{bp} - S_{cp} - 2S_{an} + S_{bn} + S_{cn})V_d$$

$$V_{ds} = 1/2\sqrt{3}(S_{cp} - S_{bp} - S_{cn} + S_{bn})V_d$$

$$V_{os} = 1/6(S_{ap} + S_{bp} + S_{cp} - S_{an} - S_b + V_{on} - S_{cn})V_d = V_{pn} \qquad (4)$$

When the three-phase voltage set is balanced, $V_o$ is zero and $V_{os}$ is equal to $V_{pn}$.

In the direct digital PWM method, the complex plane stationary reference frame qd output voltage vector of the three-phase voltage source inverter is used to calculate the turn-on times of the inverter switching devices required to

**Table I: Switching modes of the three-phase voltage source inverter and corresponding stationary reference frame qdo voltages.**

| Mode | $S_{ap}$ | $S_{bp}$ | $S_{cp}$ | $V_{qs}$ | $V_{ds}$ | $V_{os}$ |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | $-V_d/2$ |
| 2 | 0 | 0 | 1 | $-V_d/\sqrt{3}$ | $V_d/\sqrt{3}$ | $-V_d/6$ |
| 3 | 0 | 1 | 0 | $-V_d/3$ | $-V_d/\sqrt{3}$ | $-V_d/6$ |
| 4 | 0 | 1 | 1 | $-2V_d/3$ | 0 | $V_d/6$ |
| 5 | 1 | 0 | 0 | $2V_d/3$ | 0 | $-V_d/6$ |
| 6 | 1 | 0 | 1 | $V_d/3$ | $-V_d/\sqrt{3}$ | $V_d/6$ |
| 7 | 1 | 1 | 0 | $V_d/3$ | $V_d/\sqrt{3}$ | $V_d/6$ |
| 8 | 1 | 1 | 1 | 0 | 0 | $V_d/2$ |

synthesize a reference three-phase balanced voltage set. In general, the three-phase balanced voltages expressed in the stationary reference frame; situated in the appropriate sector in Figure 1(b) are approximated by the time-average over a sampling period (converter switching period, $T_s$) of the two adjacent active qd voltage inverter vectors and the two zero states $U_0$ and $U_7$. The switching turn-on times of the two active and two null states are utilized to determine the duty cycle information to program the active switch gate signals [7]. When the inverter is operating in the linear modulation region, the sum of the times the two active switching modes are utilized is less than the switching period; in which case the remaining time is occupied by using the two null vectors, $U_0$ and $U_7$. If the normalized times (with respect to modulator sampling time or converter switching period, $T_s$) the set of four voltage vectors $V_{qda}$ , $V_{qdb}$, $V_{qd0}$, $V_{qd7}$ are called into play are $t_a$ , $t_b$, $t_0$, $t_7$ respectively, then the q and d components of the reference voltage $V_{qd}^*$ are approximated as :

$$V_{qd}^* = V_{qq} + jV_{dd} = V_{qda}t_a + V_{qdb}t_b + V_{qd0}t_0 + V_{qd7}t_7$$

$$t_c = t_0 + t_7 = 1 - t_a - t_b \qquad (5)$$

When separated into real and imaginary parts, (5) gives the expressions for $t_a$ and $t_b$ as :

$$t_a = \nabla\,[\,V_{qq}V_{db} - V_{dd}V_{qb}]$$

$$t_b = \nabla\,[\,V_{dd}V_{qa} - V_{qq}V_{da}]$$

$$\nabla = [\,V_{db}V_{qa} - V_{qb}V_{da}]^{-1} \qquad (6)$$

It is observed that both $V_{qd0}$ and $V_{qd7}$ do not influence the values of $t_a$ and $t_b$ . The times $t_a$ and $t_b$ are given in Table II for voltage references in the six sectors.
It turns out that the expressions for the normalized times ($t_a$,$t_b$) displayed in Table II can be generalized as :

$$t_a = 1.5V[\cos\xi - 1/\sqrt{3}\sin\xi]$$

$$t_b = \sqrt{3}V\sin\xi \qquad (7)$$

where,
$V = \text{Abs}\,(V_{qd}^*) / V_d$, $\gamma = \text{angle}\,(V_{qd}^*)$ and $\gamma = 60(n-1) + \xi$.

**Table II : Device Switching times expressed in terms of qd reference voltage**

| Sector | I | II | III | IV | V | VI |
|---|---|---|---|---|---|---|
| $t_a$ | $0.5(3V_{qq} - \sqrt{3}V_{dd})/V_d$ | $0.5(3V_{qq} + \sqrt{3}V_{dd})/V_d$ | $\sqrt{3}V_{dd}/V_d$ | $0.5(-3V_{qq} + \sqrt{3}V_{dd})/V_d$ | $0.5(-3V_{qq} - \sqrt{3}V_{dd})/V_d$ | $-\sqrt{3}V_{dd}/V_d$ |
| $t_b$ | $\sqrt{3}V_{dd}/V_d$ | $0.5(-3V_{qq} + \sqrt{3}V_{dd})/V_d$ | $-0.5(3V_{qq} + \sqrt{3}V_{dd})/V_d$ | $-\sqrt{3}V_{dd}/V_d$ | $0.5(3V_{qq} - \sqrt{3}V_{dd})/V_d$ | $0.5(3V_{qq} + \sqrt{3}V_{dd})/V_d$ |

The integer n = 1,2,3,4,5,6 is the sector number the reference voltage is located.

To implement the space vector PWM given the reference $qd^*$ voltage, the sector is determined, and (7) is used to determine the relative switching periods of the active modes. Then the remaining time $t_c$ is shared between the two null modes respectively as $t_0 = \alpha\, t_c$ , and $t_7 = (1-\alpha)\, t_c$ where $0 \le \alpha \le 1.0$.

### III. A NON- SINUSOIDAL PWM SCHEME

In order to prevent short-circuiting the inverter DC source and thereby violate the Kirchoff's voltage law, $\mathbf{T_{ip}}$ and $\mathbf{T_{in}}$ cannot be turned on at the same time. Hence, Kirchoff's voltage law constraints the existence functions such that $\mathbf{S_{ip}} + \mathbf{S_{in}} = 1$, which when substituted in (1) are expressed as :

$$0.5\, V_d\, (2S_{ap} - 1) = 0.5\, V_d\, M_{ap} = V_{ap} + V_{pn}$$

$$0.5\, V_d\, (2S_{bp} - 1) = 0.5\, V_d\, M_{bp} = V_{bp} + V_{pn} \qquad (8)$$

$$0.5\, V_d\, (2S_{cp} - 1) = 0.5\, V_d\, M_{cp} = V_{cp} + V_{pn}$$

The voltage equations expressed in terms of the modulation signals in (8) are facilitated by the Fourier series approximation of the existence functions which are approximated as [12-13]:

$$S_{ap} \cong Z_{ap} = 0.5\,(1 + M_{ap})$$

$$S_{bp} \cong Z_{bp} = 0.5\,(1 + M_{bp})$$

$$S_{cp} \cong Z_{cp} = 0.5\,(1 + M_{cp}) \qquad (9)$$

where, $M_{ap}$ , $M_{bp}$, $M_{cp}$ which range between –1 and 1 (for the linear modulation range) are the carrier-based modulation waveforms comprising of fundamental frequency components. The approximate existence functions ($Z_{ap}$, $Z_{bp}$, $Z_{cp}$) which range between zero and unity can be used to generate actual existence functions by comparing them with a high frequency triangular waveform that ranges between unity and zero. In general, the existence functions are usually generated by comparing the high frequency triangle waveform which ranges between –1 and 1 with the modulation waveforms ($M_{ap}$, $M_{bp}$, $M_{cp}$). Hence the inverter switching signals which are connected to the base drives of the switching devices for the carrier-based PWM scheme can be achieved by either of these two methods. The equations for the modulating signals of the top devices from (8) are expressed as :

$$M_{ip} = V_{ip}/0.5\, V_d + V_{pn}/0.5\, V_d \qquad i = a,b,c \qquad (10)$$

The neutral voltage $V_{pn}$ averaged over the switching period $T_s$ is given as :

$$\langle V_{pn} \rangle = V_{oa} t_a + V_{ob}\, t_b + V_{o0}\, t_0 + V_{o7}\, t_7 \qquad (11)$$

It should be noted that $t_c$ is partitioned into dwell times for the two null voltage vector - $t_c\alpha$ for $U_o$ and $t_c(1-\alpha)$ for $U_7$. The averaged zero sequence voltages for reference voltages in the voltage sectors in Figure 1(b) calculated using (11) are shown in Table III. Table IV is the same as Table II but the expressions for the times are expressed in terms of the line-line reference voltages.

**Table III : Average zero sequence voltage for the sectors**

| Sectors | I, III, V | II, IV, VI |
|---|---|---|
| $\langle V_{pn} \rangle$ | $V_d\,(t_b - t_a)/6 + V_d\,(1-2\alpha)t_c/2$ | $V_d\,(t_a - t_b)/6 + V_d\,(1-2\alpha)t_c/2$ |

**Table IV : Device Switching times expressed in terms of reference line-line voltages**

| Sector | I | II | III | IV | V | VI |
|---|---|---|---|---|---|---|
| $t_a$ | $V_{ac}/V_d$ | $V_{ab}/V_d$ | $V_{cb}/V_d$ | $V_{ca}/V_d$ | $V_{ba}/V_d$ | $V_{bc}/Vd$ |
| $t_b$ | $V_{cb}/V_d$ | $V_{ca}/V_d$ | $V_{ba}/V_d$ | $V_{bc}/V_d$ | $V_{ac}/V_d$ | $V_{ab}/V_d$ |
| Max Volt | $V_{ap}$ | $V_{bp}$ | $V_{bp}$ | $V_{cp}$ | $V_{cp}$ | $V_{ap}$ |
| Min Volt | $V_{cp}$ | $V_{cp}$ | $V_{ap}$ | $V_{ap}$ | $V_{bp}$ | $V_{bp}$ |

Substituting the expressions for the dwell times given in Table IV into the expressions for the averaged zero sequence voltages in Table III, the generalized expression for the averaged neutral voltages in all the six sectors is given in (12). Substituting (12) into (10), the expressions for the modulation signals are shown in (13).

$$V_{pn} = 0.5V_d\,(1-2\alpha) - \alpha V_{min} + V_{max}\,(\alpha - 1) \qquad (12)$$

$$M_{ip} = V_{ip}/0.5V_d + (1-2\alpha) - \alpha V_{min}/0.5V_d + V_{max}\,(\alpha-1)/0.5V_d \qquad (13)$$

In (13) $V_{max}$ and $V_{min}$ are the instantaneous maximum and minimum magnitudes of the three reference balanced phase

voltages, respectively. Equation (13) which first appeared in [9] and determined using a different method is what has given rise to what is known as the Hybrid PWM (HPWM) and later described as a non-sinusoidal PWM scheme [10-11]. In the implementation of this modulation scheme $\alpha$ can take any form (constant or time-varying) ranging between zero and unity. [9-11]. The choice of parameter $\alpha$ affects the neutral voltage between the load star-point and the inverter reference. In the conventional space vector modulation, $\alpha$ is generally taken as 0.5. However; other functions may be used, which improve the performance of the modulator. The selection of $\alpha$ gives rise to an infinite number of carrier-based PWM modulations, some of which have been discovered [5-11].

## IV. THE GENERALIZED DISCONTINUOUS MODULATION SCHEME

This section presents a discontinuous modulation technique which is applicable to both star and delta connected three-phase loads. The expressions for the discontinuous modulation signals for the devices are determined by averaging their existence functions in each space vector sector. Figure 2 shows the existence functions of the three top devices of the inverter when operating in the first sector. These existence functions are obtained by using the Sequence 111→110→100→000→000→100→110→111. It is observed from Fig. 2 that the average (the first term of the Fourier series expansion) of an existence function is equal to the sum of the normalized times each device is turned on to realize a reference voltage. Based on Tables I and II and (5), the total normalized time each top device is turned on for the six sectors are listed in Table V. These times using Table IV expressed in terms of the normalized reference phase voltage, are given in Table VI. These expressions are equivalent to the normalized modulation signals for the top devices. Note that $0 \le \beta = (1- \alpha) \le 1$ which when varied introduces different weights to the times the null switching modes are used.

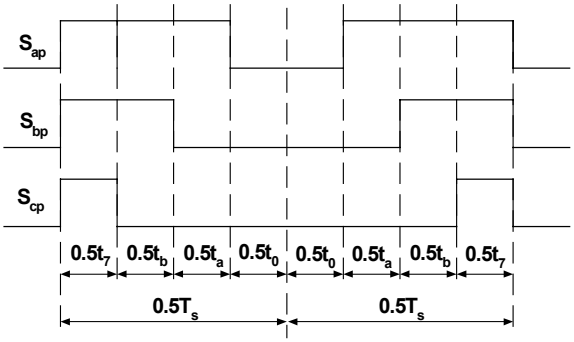



Figure 2 : Existence functions of top devices for operation in sector I

When $\beta = 1$, each top inverter leg connected to a phase is clamped to the upper rail of the DC source for 120 degrees and the lower inverter leg is clamped to the lower rail of the DC source when $\beta = 0$ . Various kinds of GDPWM waveforms which have been reported in the literature including DPWMIN, DPWMMAX, DPWM1, DPWM2, and DPWM3 can be generated using either equation (13) or Table VI for an inverter feeding a star-connected load and Table VII for the inverter actuating the delta connected load. When $\beta = 0$ and $\beta = 1$, DPWMMAX and DPWMMIN are obtained, respectively and $\beta = 0.5$, gives the SVPWM as shown in figure 3. With the definition $\beta = 0.5[1 + \text{Sgn}(\text{Cos } 3(\omega t + \delta))]$ where $\omega$ is the angular frequency of the reference voltage and $\delta$ is the modulation phase angle, an infinite number of modulation waveforms can be generated. If $\delta = 0, -\pi/6, -\pi/3$, the resulting modulation signals are the same as the DPWM1, DPWM2, and DPWM3 respectively as illustrated in fig. 4.

**Table V : Normalized times devices the three top devices are turned on**

| Sector | I | II | III | IV | V | VI |
|---|---|---|---|---|---|---|
| $\tau_{ap}$ ($Z_{ap}$) | $t_a + t_b + t_7$ | $t_a + t_7$ | $t_7$ | $t_7$ | $t_b + t_7$ | $t_a + t_b + t_7$ |
| $\tau_{bp}$ ($Z_{bp}$) | $t_b + t_7$ | $t_a + t_b + t_7$ | $t_a + t_b + t_7$ | $t_a + t_7$ | $t_7$ | $t_7$ |
| $\tau_{cp}$ ($Z_{cp}$) | $t_7$ | $t_7$ | $t_b + t_7$ | $t_a + t_b + t_7$ | $t_a + t_b + t_7$ | $t_a + t_7$ |

**Table VI : Discontinuous existence functions for top devices with star-connected load, $V_{iin} = V_{ij}/V_d$ , where i, j = a,b,c and $i \neq j$ . ( $\beta = 1- \alpha$)**

| Sector | $Z_{ap}$ | $Z_{bp}$ | $Z_{cp}$ |
|---|---|---|---|
| VI | $\beta(1-V_{acn}) + V_{acn}$ | $\beta(1-V_{acn}) + V_{bcn}$ | $\beta(1-V_{acn})$ |
| V | $\beta(1-V_{bcn}) + V_{acn}$ | $\beta(1-V_{bcn}) + V_{bcn}$ | $\beta(1-V_{bcn})$ |
| IV | $\beta(1-V_{ban})$ | $\beta(1-V_{ban}) + V_{ban}$ | $\beta(1-V_{ban}) + V_{can}$ |
| III | $\beta(1-V_{can})$ | $\beta(1-V_{can}) + V_{ban}$ | $\beta(1-V_{can}) + V_{can}$ |
| II | $\beta(1-V_{cbn}) + V_{abn}$ | $\beta(1-V_{cbn})$ | $\beta(1-V_{cbn}) + V_{cbn}$ |
| I | $\beta(1-V_{abn}) + V_{abn}$ | $\beta(1-V_{abn})$ | $\beta(1-V_{abn}) + V_{cbn}$ |

## V. MODULATION FOR UNBALANCED VOLTAGES

There are situations in which it is desirable to impress an unbalanced three-phase voltage set to an unbalanced three-phase load in order to ensure a balanced three-phase load current or to use unbalanced three-phase voltage set for voltage or current compensation in active filters in distribution lines. In general, four-leg inverters are used in such applications since the phase currents are not constrained when the load is star-connected. However; when the impressed unbalanced three-phase voltage set is constrained such that the load currents add to zero in star-connected loads, a three-leg inverter can be used. Under such conditions, the expressions for the three modulation signals $M_{ip}$ from (10) must be determined given the phase voltages $V_{an}$ , $V_{bn,}$ $V_{cn}$ which are not balanced in general. Since there are three linear independent equations to be solved to determine expressions for three unknown modulation signals and $V_{pn}$, these equations are under-

determined. In view of this indeterminacy, there is an infinite number of solutions which are obtained by various optimizing performance functions defined in terms of the modulation functions. For a set of linear indeterminate equations expressed as AX = Y, a solution which minimizes the sum of squares of the variable X is obtained using the Moore-Penrose inverse [14]. The solution is given as $X = A^T[AA^T]^{-1}Y$. The solution is for the minimization of the sum of the squares of the three modulation signals and the square of the normalized neutral voltage ($V^*_{pn} = V_{pn}/0.5\ V_d$). Equivalently, this is the maximization of the inverter output-input voltage gain, i.e. $M_{ap}^{\ 2} + M_{bp}^{\ 2} + M_{cp}^{\ 2} + V^*_{pn}{}^2$ subject to the constraints in (1). The result expressions for the modulation signals are given as :

$$M_{ap} = 1/4\ (3V_{ann} - V_{bnn} - V_{cnn})\ ,\ V_{ann} = V_{an}/\ 0.5V_d$$

$$M_{bp} = 1/4\ (-V_{ann} + 3V_{bnn} - V_{cnn})\ ,\ V_{bnn} = V_{bn}/\ 0.5V_d$$

$$M_{cp} = 1/4\ (-V_{ann} - V_{bnn} + 3V_{cnn})\ ,\ V_{cnn} = V_{cn}/\ 0.5V_d$$

$$V^*_{pn} = 1/4\ (-V_{ann} - V_{bnn} - V_{cnn}) \qquad (14)$$

An alternative carrier based discontinuous modulation scheme is obtained by using the Space Vector methodology to determine the expression for $V_{pn}$ in (10). Since the reference voltage set is unbalanced, the reference three-phase voltages mapped to the stationary reference frame has in addition to the q and d voltage components the zero sequence voltage. The reference zero sequence voltage, $V_o$ is approximated by time-averaging the zero sequence voltages of the two active and two null modes. From (4), the neutral voltage $V_{pn}$ averaged over the switching period $T_s$ is given as :

$$\langle V_{pn} \rangle = V_{oa}t_a + V_{ob}\,t_b + V_{o0}\,t_0 + V_{o7}\,t_7 - V_o \qquad (15)$$

Table VIII gives the expression for the averaged neutral voltage $\langle V_{pn} \rangle$ for the six sectors of the space vector.
Hence, given the unbalanced voltage set at any instant, $V^*_{qdo}$ in the stationary reference frame is found and the sector in which $V^*_{qd}$ is located is determined. The expression for $V_{pn}$ is then selected and is subsequently used in (10) to determine the modulation signals for the three top devices.

**Table VIII : Expressions for the neutral voltage for the six sectors**

| Sector | Neutral Voltage $\langle V_{pn} \rangle$ |
|---|---|
| VI | $(2V_b - V_a - V_c)/6 + 0.5V_d\,(1-2\alpha) + 0.5\,(1-2\alpha)[V_c - V_a]$ |
| V | $(2V_a - V_b - V_c)/6 + 0.5V_d\,(1-2\alpha) + 0.5\,(1-2\alpha)[V_c - V_b]$ |
| IV | $(2V_c - V_a - V_b)/6 + 0.5V_d(1-2\alpha) + 0.5\,(1-2\alpha)[V_a - V_b]$ |
| III | $(2V_b - V_a - V_c)/6 + 0.5\ V_d(1-2\alpha) + 0.5\ (1-2\alpha)[V_a - V_c]$ |
| II | $(2V_a - V_b - V_c)/6 + 0.5V_d\,(1-2\alpha) + 0.5\,(1-2\alpha)[V_b - V_c]$ |
| I | $(2V_c - V_a - V_b)/6 + 0.5\ V_d(1-2\alpha) + 0.5\,(1-2\alpha)[V_b - V_a]$ |

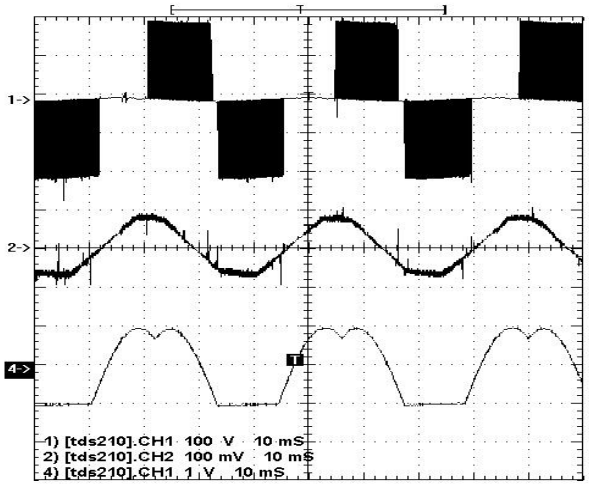
## VI. EXPERIMENTAL AND SIMULATION RESULTS

Illustrative experimental results are given in Figures 3 and 4 showing the nature of the discontinuous modulation waveforms and the corresponding voltage and current waveforms when an unloaded induction machine is fed with a voltage source inverter under various types of generalized discontinuous modulation. In these figures, the relationships between the modulation schemes derived in this paper and those already reported in the literature are established. In particular, Figure 4 shows how the change in the values of the so-called modulation angle $\delta$ in the expression for the partition quotient $\beta$ influences the modulation waveforms with the significant implication that the modulation signal of a phase has at least one segment which is clamped to either the positive or negative rail for a total of 120 degrees.

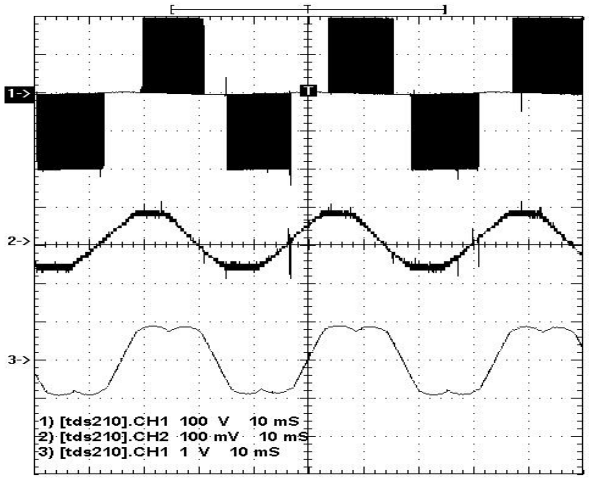
Finally, Figures 5 shows the simulation results of an inverter feeding an unbalanced load with the desired objective of balancing the load current. The resistances of the R-L load used are $r_a = 0.5$ Ohm, $r_b = 0.5$ Ohm, $r_c = 0.5$ and the corresponding load inductances are $L_a = 0.025$H, $L_b = 0.02$H, $L_c = 0.0125$H. With given reference three-phase currents, the corresponding phase voltages are determined and used in equations (14) to realize the continuous modulation signals which are subsequently used to generate the required voltages. In fig. 5 both the balanced reference phase currents are shown to effectively track the actual phase currents brought about by the line-line voltages shown in fig. 5(c-d). The same balanced current set can be generated by using the discontinuous modulation scheme based on Table VIII and (10). With $\beta = 0.5[1 + \mathrm{Sgn}(\cos 3(\omega t + \delta))]$ where $\beta = 1 - \alpha$ , fig 6 is generated for values of $\delta = 0°, -30°, -60°$. It is observed that devices are clamped to the positive or negative rail for less than 120 degrees unlike when the phase voltages are balanced in Fig 4. .

## VII. CONCLUSION

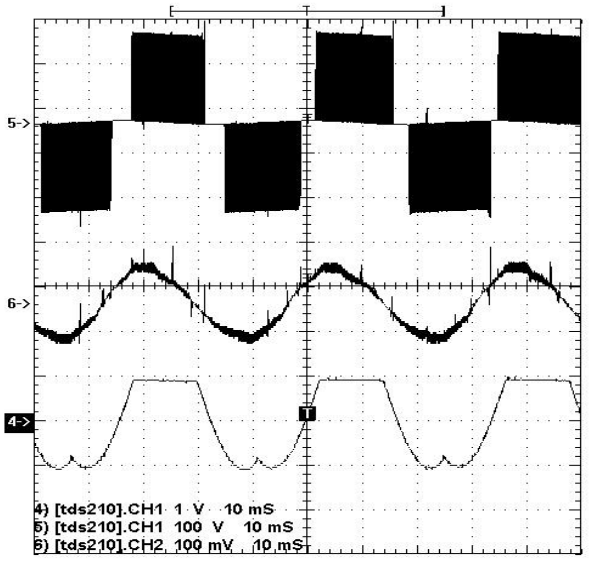
This paper presents an analytical methodology for the determination of the expressions for the modulation signals required in carrier-based generalized discontinuous PWM modulation schemes in three-phase inverters. We have generalized and clarified the methods for arriving at the modulation schemes of converters in the process of which several known modulation schemes have been brought under a unifying and easy-to- understand theory. The proposed scheme for evolving modulation strategies is applicable to star and delta connected loads and for situations where the reference three-phase voltages are either balanced or unbalanced. This development is made possible with the extension of the classical space vector




(a)

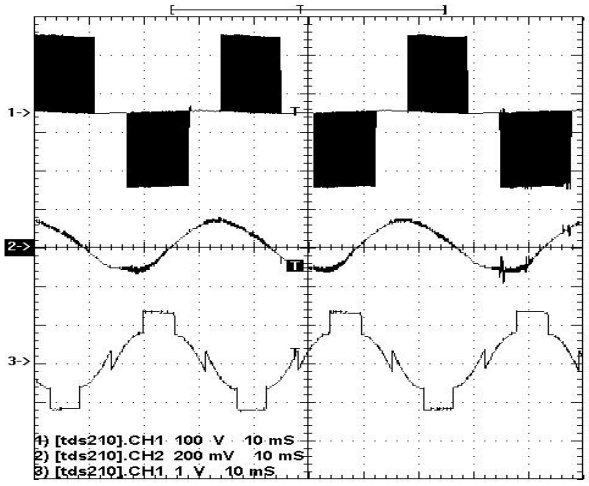



(b)

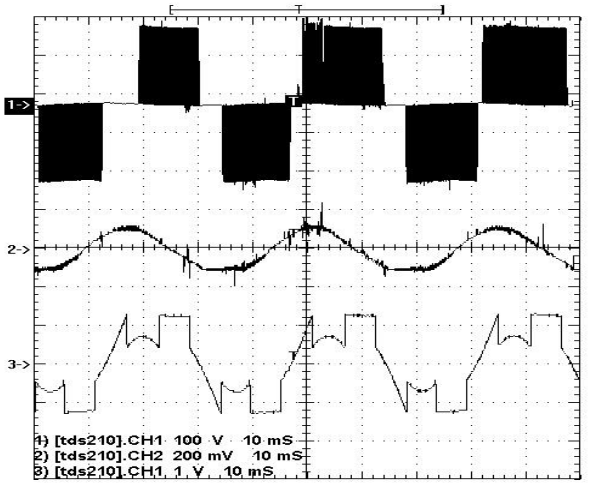



(c)

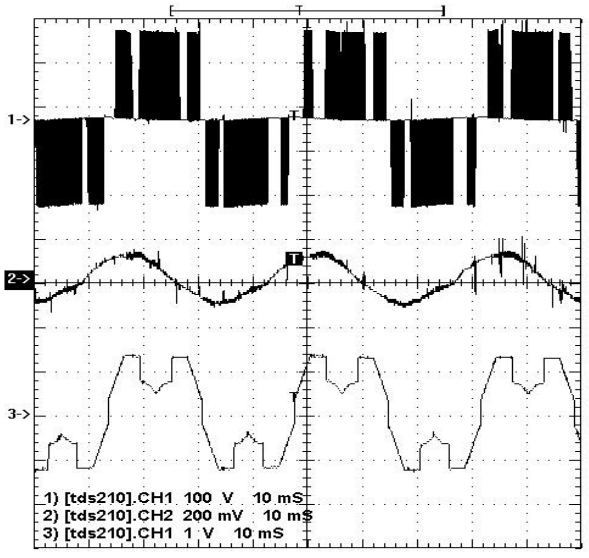
Figure 3: Experimental results for three-phase inverter under GDPWM modulation feeding an induction motor on no-load. $V_d$ = 200V, frequency = 30 Hz., Modulation magnitude = 0.9 (1) Motor line-line voltage, (2) motor phase current. (a) β = 0, DPWMMAX,(b) β = 0.5, SVPWM, (c) β =1.0., DPWMMIN.




(a)




(b)




(c)

Figure 4: Experimental results for three-phase inverter under GDPWM modulation feeding an induction motor on no-load. $V_d$ = 200V, frequency = 30 Hz, modulation magnitude = 0.9 (1) motor line-line voltage, (2) motor phase current. β = 0.5[1 + SgnCos 3(ωt + δ)] , (a) δ = 0, DPWM1,(b) δ = -30°, DPWM2, (c) δ = -60°, DPWM3.

technique and the appropriate definition of the distribution or partition ratio of the times the zero (null) switching modes are used in the synthesis of a reference voltage. Some confirmatory experiments results have been provided to illustrate the various generalized carrier-based modulation signals possible. The methodology is extendable to the determination of discontinuous modulation schemes of other converters such as four-leg, multi-level, AC-AC and other variants.

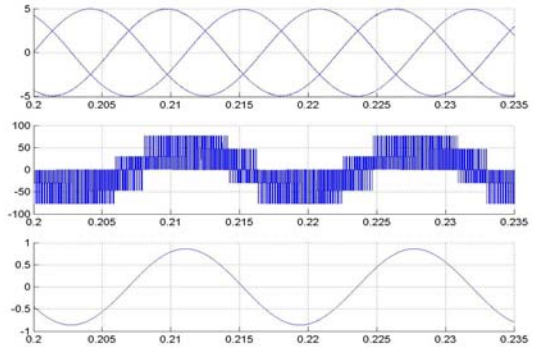


Figure 5: Balanced current in an unbalanced load. Reference peak current is 5A. (a) Balanced three phase actual currents (b) Phase a volatege, (c) Modulating signal.

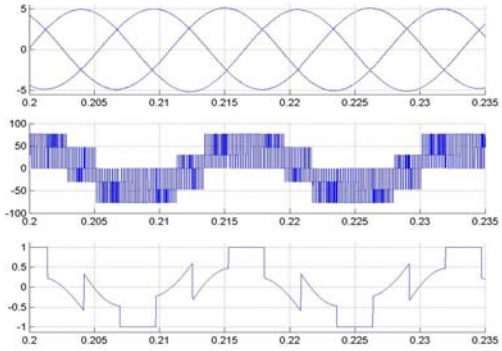


Figure 6 : Simulation results for unbalanced three-phase voltage under GDPWM. $\beta = 0.5[1 + \text{SgnCos } 3(\omega t + \delta)]$ , $\delta = 0$, DPWM1,(a) Balanced three-phase current (b) phase a voltage Vas (c) Modulation signal.

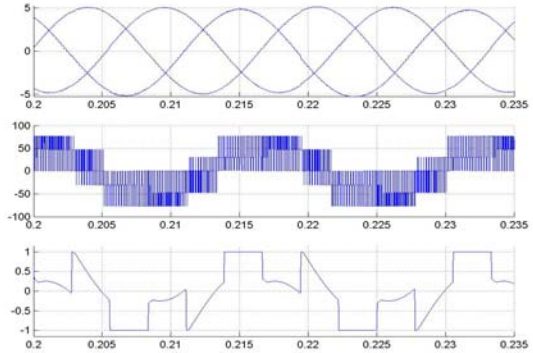


Figure 7 : Simulation results for unbalanced three-phase voltage under GDPWM. $\beta = 0.5[1 + \text{SgnCos } 3(\omega t + \delta)]$ , $\delta = -30$, DPWM2,(a) Balanced three-phase current (b) phase a voltage Vas (c) Modulation signal.

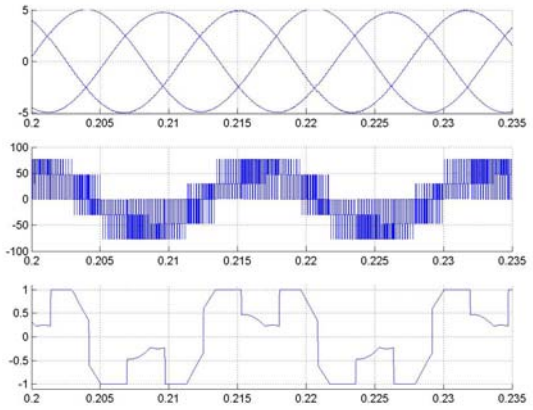


Figure 8 : Simulation results for unbalanced three-phase voltage under GDPWM. $\beta = 0.5[1 + \text{SgnCos } 3(\omega t + \delta)]$ , $\delta = -60$, DPWM3,(a) Balanced three-phase current (b) phase a voltage Vas (c) Modulation signal.

## REFERENCES


[1] A. Schonug and H. Stemmler, "Static Frequency Changers with Subharmonic Control in Conjunction with Reversible Variable Speed AC Drives," *Brown Boveri Review*, pp. 555-577, September 1964.

[2] A. Hava, R. J. Kerkman and T. A. Lipo, " Simple Analytical and Graphical Methods for Carrier based PWM VSI Drives, *IEEE Trans. on Power Electronics*, vol. 14, no. 1, pp. 49-61, January 1999.

[3] A. Hava, R. J. Kerkman and T. A. Lipo, "A High Performance Generalized Discontinuous PWM Algorthim," *IEEE Trans. On Industry Applications*, vol. 34, no. 5, pp. 1059-1071, September/October 1998.

[4] B. K. Bose, **Power Electronics and Variable Frequency Drives, Technology and Applications**, IEEE Press, New York, 1997.

[5] J. Holtz, " Pulse-width modulation for Electronic Power Conversion," *Proceedings of the IEEE*, vol. 8, pp. 1194-1214, August 1994.

[6] B. K. Bose, **Modern Power Electronics and AC Drives**, Prentice-Hall,Upper Saddle River, New Jersey, 2002.

[7] H. Van Der Broeck, H. Skudelny and G. Stanke, "Analysis and Realization of a Pulse Width Modulator Based on Voltage Space Vectors," *IEEE Trans. on Industry Applications*, Vol. IA-24, No. 1, pp. 142-150, January 1988.

[8] S. Ogasawa, H. Akagi, and A. Nabae, "A Novel PWM Scheme of Voltage Source Inverter Based on Space Vector Theory," *European Power Electronics Conference*, Aachen, Germany, pp. 1197-1202, Oct. 1989.

[9] Vladimir Blasko, "Analysis of a Hybrid PWM Based on Modified Space Vector and Triangle Comparison Methods," *IEEE Trans. on Industry Applications*, Vol. 33, No. 3, pp. 756-764, May/June 1997.

[10] C. B. Jacobina, A. M. Lima, E. Da Silva, " Digital Scalar Pulse-Width Modulation : A Simple Approach to Introduce Non-Sinusoidal Modulating Waveforms," IEEE Trans. on Power Electronics, Vol. 16. No. 3, pp. 351-359, May 2001.

[11] K. Zhou and D. Wang, "Relationship between Space Vector Modulation and three-Phase Carrier-Based PWM : A Comprehensive Analysis," *IEEE Trans. on Industrial Electronics*, vol. 49, no. 1, pp. 186-196, February 2002.

[12] R. Erickson and D. Maksimovic, **Fundamentals of Power Electronics**, Kluwer Academic Publishers, Norwell, USA, 2001.

[13] P. Wood, **Switching Power Converters**, Van Nostrand Reinhold Company, New York, 1981.

[14] R. Stengel, **Stochastic Optimal Control**, John Wiley, New York, 1986.