CHAPTER 10

HARDWARE IMPLEMENTATION

This section of the chapter presents the design details of the three level diode clamped inverter .In the laboratory a three-level diode clamed inverter prototype is being built. The primary purpose of the prototype is to verify the analytical and control algorithms that are developed in this thesis. The prototype built is flexible and robust enough to conduct the experiments. The prototype can be used both as an inverter and also as the rectifier. There are several steps involved in implementing the hardware.

- Inverter design.
- DSP coding using the code composer studio.
- Building the voltage sensors to sense the capacitor voltages.
- Building the current sensors to sense the input node currents and the phase currents.

10.1 Inverter Design

10.1.1 Construction of a Three Phase Three level Diode Clamped Inverter

Specifications:

1. Voltage rating 200Vdc input.
2. Current rating 5 A.
3. Switching frequency < 50KHz (5KHz).

4. All the devices in the inverter are isolated and have separate driving circuits.

Assumptions:

- It is inferred that for this particular case, short circuit protection and overload protection are not mandatory.
- The control signals for this inverter are through an external source like DSP or micro-controller or any other PWM generation IC.

The important tasks in the implementation of the inverter are building the power circuit, building driving circuit board, and to build the power supplies for the driver circuits. Selection of the power devices and the clamping diodes is also an important criterion.

10.2 Power Circuit

In building the power circuit of the three-level inverter, 12 switching devices and six clamping diodes, two capacitors, a dc source, gate driver circuit board, power supply to the circuit boards.

10.2.1 Selection of IGBT

IGBTs have been the preferred device under these conditions:

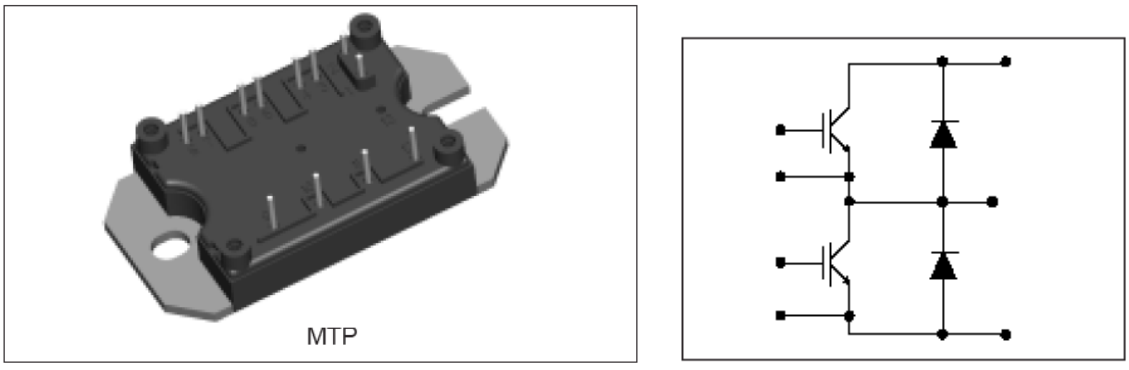
- Low duty cycle
- Low frequency (<20kHz)

- Narrow or small line or load variations
- High-voltage applications (>1000V)
- Operation at high junction temperature is allowed (>100°C)
- >5kW output power

Rating of the switching device

The switching device considered in building the power stage is 50MT060WH, a product of the IRF Rectifier is shown in Figure 10.1.

- Since the voltage that is impressed in the present case is around 200 V and considering a factor of 3, the voltage rating of the device is selected as 600V.
- The allowable current that the device must handle is around 5 A and hence considering a factor of 3, the device with a current rating of 15 A is selected. Due to the unavailability of the device with this current rating, a device with 50 A is considered.



(I) (II)

Figure 10.1: (I) IGBT module (50MT060WH) (II) Schematic of the IGBT module.

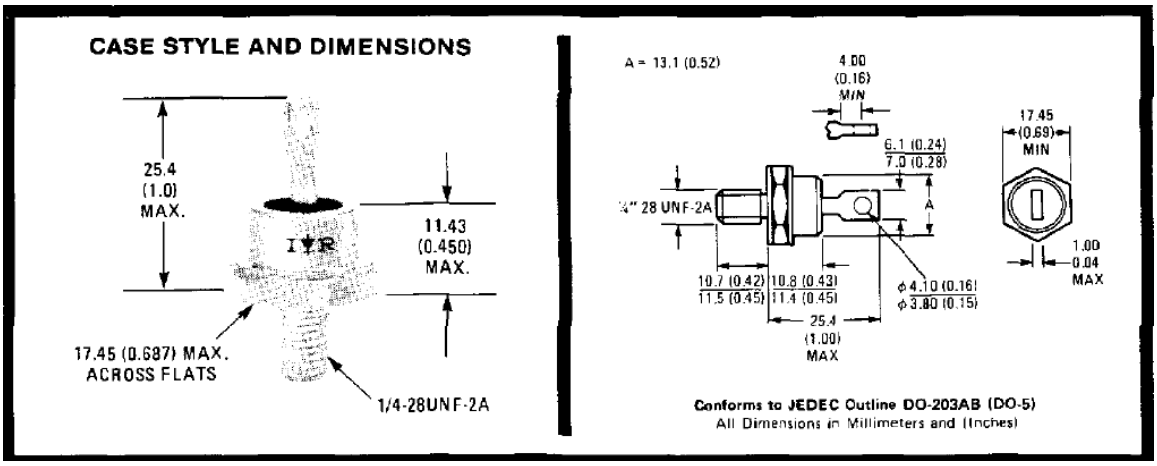


Figure 10.2: Picture of the power diode.

10.2.2 Power Diodes

The main function power diodes used in building the circuit of the three-level inverter is to clamp the dc bus voltage. In case of three level inverter, the diodes have to clamp half the dc-link voltage and hence the diode has to clamp a voltage of 100 V in the present case and considering a factor of three, a diode with rating of 300 V and a current rating of 15 A is considered. Figure 10.2 shows the power diode that has been used.

10.2.3 Power Supplies

In implementing the inverter, the power supplies have to isolate from each other, i.e., having separate grounds. By having separate isolated power supplies for the gate drives, any dv/dt coupled noise generated by the power device switching stays within the gate power supply circuits. Also since there is problem of shorting of shorting between

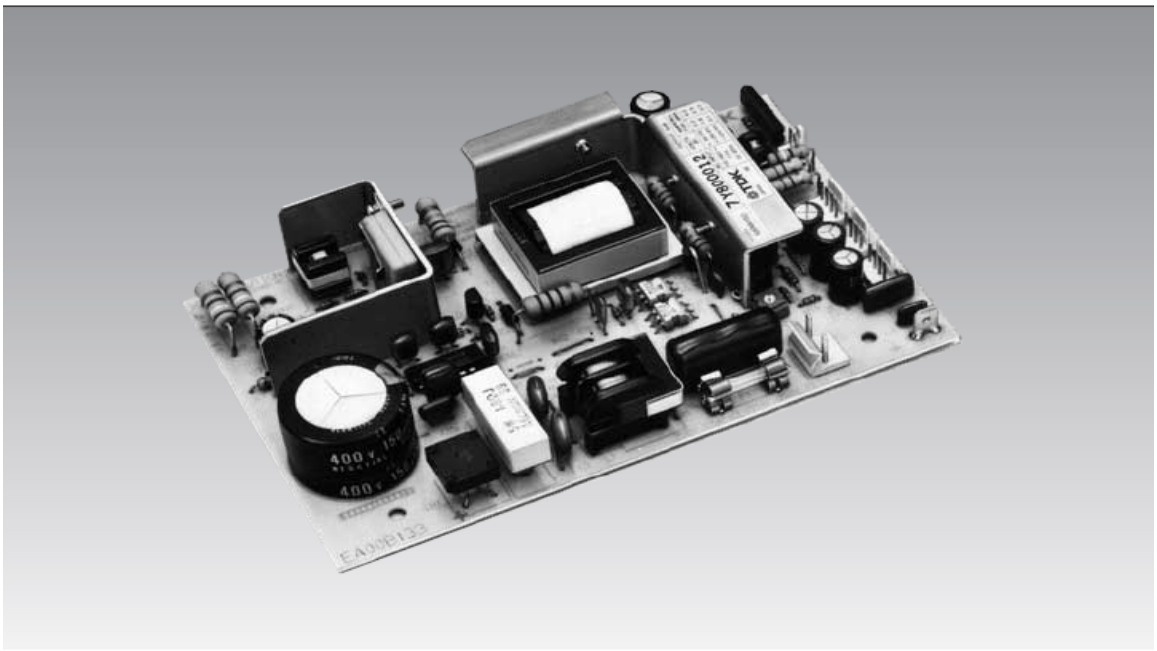


Figure 10.3: Isolated dc power supply with multiple outputs

the devices, the driver boards connected to the power switches have to be supplied with isolated power supplies to avoid the shoot through current to pass through the devices. The voltage sensors and current sensors are also supplied with different power supplies. Even the DSP has a different power supply. The picture of the power supply used is shown in Figure 10.3.

10.3 Design of Gate Drive Circuit for IGBT

The threshold gate voltage of the IGBT is around 4 V, but to ensure switching ON and OFF of the devices at higher frequencies, the gate voltage range is between +12 V and –12 V. In order to provide a sufficient gate drive current a BC547 – BC557 push-pull pair is used. These transistors are operated in saturation region. The circuit diagram of the gate drive circuit for the IGBT is shown in Figure 10.4.

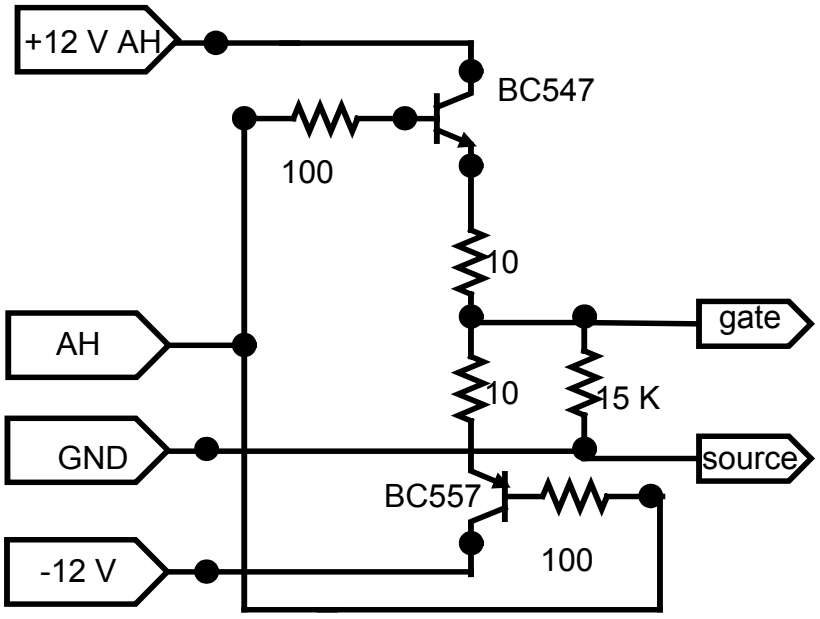


Figure 10.4: Schematic of the gate drive circuit.

10.4 Design of Opto-isolator Circuit

For providing opto-isolation between the power stage and the drive signal stage, the opto-isolator driver IC TLP 250 is used.

Following reasons justify the advantages of using TLP 250.

1. Input threshold voltage current If = 5mA (max)
2. Supply Voltage 10V-35V
3. Output Peak current 2A
4. Response speed 0.5us
5. Isolation Voltage 2500Vrms

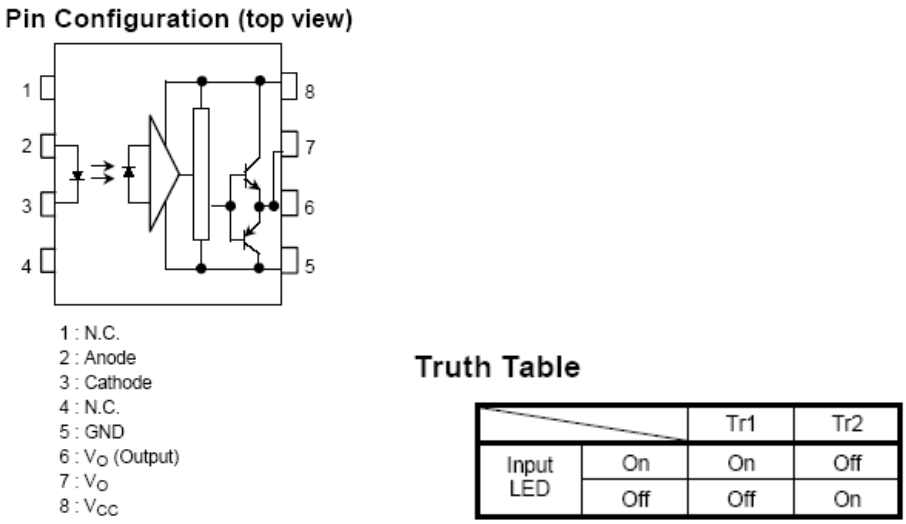


Figure 10.5: Pin configuration of the TLP250 and the truth table.

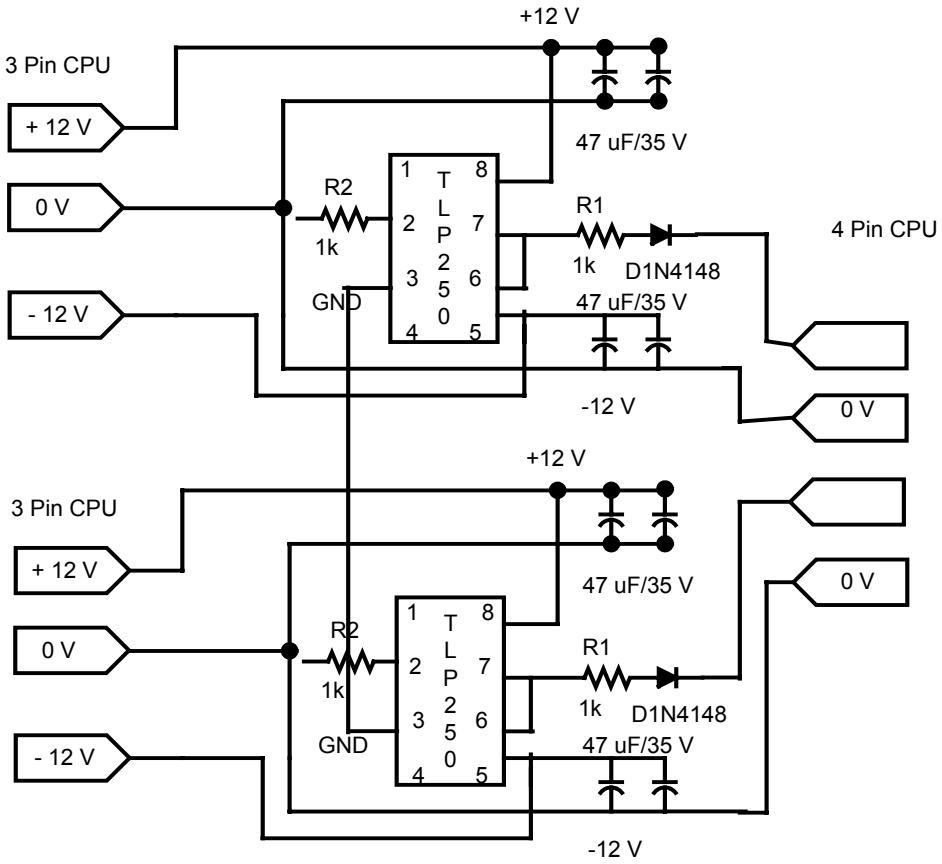


Figure 10.6: Complete circuit of a driver circuit board.

10.5 PWM Generation

TMS320LF2407 DSP is being used in the laboratory to obtain the gating signals .To obtain pulse width modulated waveforms, a triangular carrier at the switching frequency needs to be generated. The cosine and sine routine programs of the DSP generate the modulation signals and the zero sequence voltage expression is added to obtain the discontinuous modulation signals. In the DSP, the carrier-based implementation, there is no actual triangle that is being compared with the modulation signals to generate the gating signals. In each modulation cycle (triggered by the PWMSYNC interrupt service routine) the DSP must compute the new on-time value to write to the six duty cycle registers of the PWM generation unit. These on times are loaded into the compare registers of the DSP and when the timer reaches the loaded value in the compare register, a pulse of + 12 V is given out. Hence the carrier-based scheme can be implemented using the above method.

The generation of the PWM signals in case of the three-level converter is different when compared to conventional two-level converter. In the carrier-based implementation of the three-level converter, as explained PD technique is used where in two carrier waveforms are used which are displaced equally and in phase, Triangle 1 varying from +1 – 0 and Triangle 2 varying from 0 - -1, whereas in case of the two level converter only a single carrier which varies from +1 - -1 is used.

The technique in generating the two triangle waveforms is, during the comparison of the positive cycle of the modulation signal, the actual waveform is compared with the

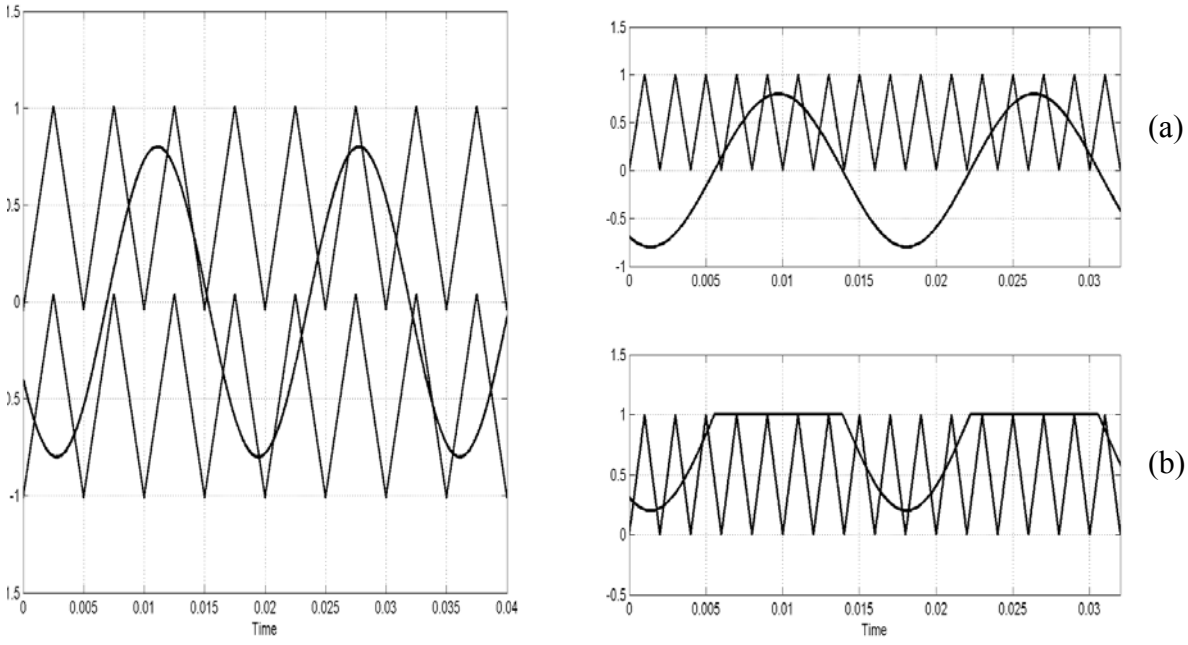


Figure 10.7: (I) Carrier-based PWM scheme using the phase disposition (II) (a) Comparison during the positive cycle of the modulation signal (b) Offset added modulation signal during the negative cycle of the signal.

Triangle 1 and during the negative modulation signal, an offset of "1" is added to the signal so that the signal goes positive and if the region of the signal which goes above "1" is clamped to 1 as shown in Figure and the using this as the modulation signals the on-times are calculated and PWM scheme is implemented.

Figure 10 .7 (I) shows the simulation of carrier-based PWM using the phase disposition technique. It shows the two carriers and a modulation signal. Figure 10.7 (II) shows the method used to implement the phase disposition technique. (a) shows the signal during the positive cycle and (b) shows the signal during the negative cycle and it can be seen that during the negative cycle, when offset is added, the signal goes beyond 1 and for all the region beyond 1 is clamped to 1 as shown in figure.

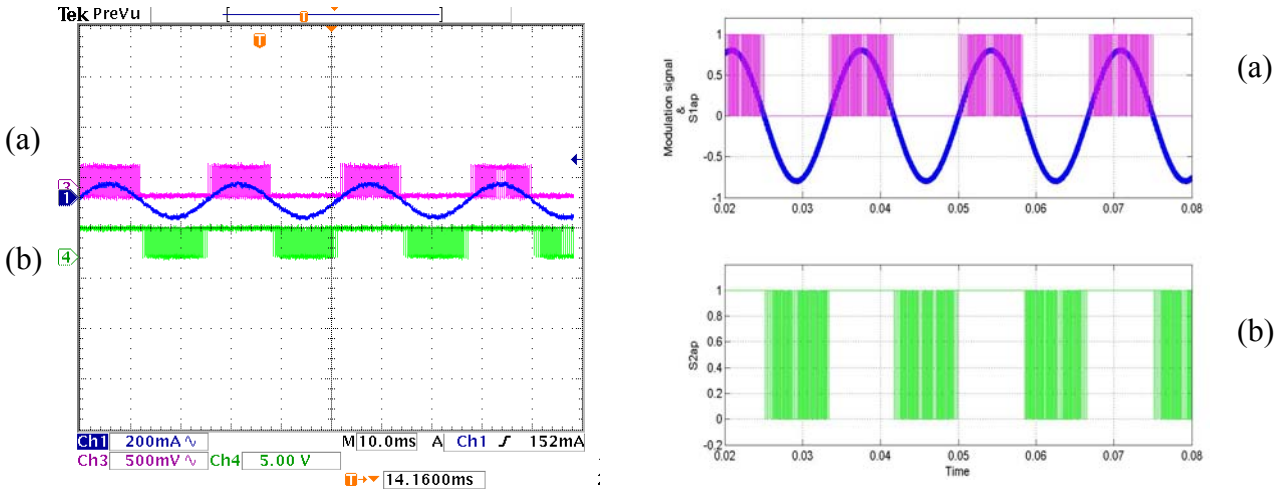


Figure 10.8: Experimental and simulation of the switching produced. (I) (a) Switching produced during the positive cycle for the top device (S_{1ap}) (b) Switching of the device (S_{2ap}).

Figure 10.8 shows the experimental and the simulation results of the switching produced using the proposed scheme, (I) (a) shows the modulation signal and the switching of the top device (S_{1ap}) and (b) shows the switching of the next device (S_{2ap}).