## BIOGRAPHICAL SKETCH

Utkarsh Dilip Kavimandan was born in Nashik, Maharashtra, India. He received a B.E. in instrumentation and control engineering from the University of Pune-affiliated institution in Nashik, Maharashtra, India, in 2012, and an M.S. degree in electrical engineering in 2016 from Wright State University, Dayton, OH, USA. He is currently working towards his Ph.D. degree in electrical engineering from the Tennessee Technological University, Cookeville, TN, USA, where he is a Graduate Research Assistant at the Center for Energy Systems Research (CESR). From August 2015 to December 2015, he interned with Ametek/Prestolite Power in Troy, OH, USA. In 2018 and 2019, he worked as an ASTRO intern in Power Electronics and Electric Machinery (PEEM) Group at Oak Ridge National Laboratory, Knoxville, TN, USA.

## EDUCATION

Doctor of Philosophy
Engineering
Tennessee Tech University, December 2021 *(expected)*
Cookeville, Tennessee

Master of Science
Electrical Engineering
Wright State University, 2016
Dayton, Ohio, United States

Bachelor of Engineering
Instrumentation and Control Engineering
University of Pune, 2012
Nashik, Maharashtra, India

College of Engineering

TENNESSEE TECH

The Department of

Electrical and Computer Engineering

Announces the Dissertation Defense of

# *Utkarsh D. Kavimandan*

In Partial

Fulfillment of the Requirements

For the degree of

Doctor of Philosophy in Engineering

October 14, 2021

8:00-9:30 a.m. CST

**Tennessee Tech University**

Location: Teams Meeting
Link: https://teams.microsoft.com/l/meetup-join/19%3ameeting_NDIyMTg0YmMtZWI3MC00OWM4LWIyZjktMmNlOGMwY2NiMzE0%40thread.v2/0?context=%7b%22Tid%22%3a%2266fecaf8-3dc0-4d2c-b8b8-eff0ddea46f0%22%2c%22Oid%22%3a%22f0466677-aa2d-450c-8c09-67da8d8007e3%22%7d

## FIELD OF STUDY

Wireless power transfer systems for electric vehicle charging application, Power electronics

## DISSERTATION TOPIC

INVESTIGATION OF INVERTER DEAD-TIME EFFECTS IN SINGLE-PHASE WIRELESS POWER TRANSFER SYSTEMS

## EXAMINING COMMITTEE

Dr. Satish M. Mahajan, Committee Chair
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## ABSTRACT

Wireless power transfer (WPT) systems have the potential to alleviate challenges associated with the existing plug-in electric vehicle (EV) charging technology, and further facilitate the penetration of EVs on a large scale. The present research is focused on developing control strategies to maintain the entire system’s rated power transfer and efficiency. However, the device and system-level implementation issues such as dead-time between the inverter phase-legs may impact the system performance, which must be studied in detail. Dead-time is the time interval during which all the inverter metal-oxide-semiconductor-field-effect-transistors (MOSFETs) are maintained in the OFF state. The energy stored in the resonant network conducts the MOSFET body-diodes resulting in unwanted distortions, which are commonly attributed as voltage polarity reversal (VPR). This dissertation provides a comprehensive analysis of the impact of inverter dead-time on the overall WPT system. The operating conditions of the WPT system inverter are identified, which generate the VPR at the inverter output. In addition, a mathematical analysis of the inverter voltage waveform is carried out using a Fourier series to evaluate the impact of dead-time on the entire WPT system. Validation of analytical results was carried out on a WPT system prototype, which shows less than 3% error between the experimental results and the theoretical analysis. Furthermore, a control scheme is proposed to mitigate the VPR by controlling the inverters’ switching frequency and phase-shift angle. The control scheme discussed in this dissertation maintains the DC output voltage of the system at a reference value and does not affect the battery charging process. A closed-loop control scheme was implemented on a piecewise linear electrical circuit simulation (PLECS). The openloop validations show a reduction in the inverter power loss by $\sim$ 40%. In addition, a proof-of-concept of a sensor-less coil detection scheme based on the exploitation of inverter VPR is also discussed. The validation of the control scheme was carried out on the PLECS circuit simulator, without any communication from the secondary side, with a marginal standby inverter power loss.